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EHF SATCOM Payload Frequency Synthesizer Study : Final Report

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ABSTRACT

This report describes the results of a detailed study into the development of an EHF SATCOM payload frequency-hopping synthesizer. The synthesizer is required to provide an output between 20.2 GHz and 21.2 GHz, in steps of up to 200 Hz, with a switching time of less than 900 nanoseconds. A literature review of the various synthesizer architectures was conducted and used to devise three possible synthesizer solutions. These three solutions were then compared on the basis of a number of key criteria. The preferred synthesizer, of the three, will provide the required output in steps of 0.92 Hz, with a switching time of 100 nanoseconds. The various characteristics of the preferred synthesizer are described in detail. The viability of implementing a design using the preferred synthesizer approach is discussed. Finally, a specification sensitivity analysis of the selected synthesizer approach is performed.

LIST OF ABBREVIATIONS and SYMBOLS

DA	Design Authority
DAC	Digital-to-Analogue Converter
DAS	Direct Analogue Synthesizer
DDS	Direct Digital Synthesizer
EHF	Extremely High Frequency
EMC	Electromagnetic Compatibility
HMIC	Hybrid Microwave Integrated Circuit
LPF	Low Pass Filter
MIC	Microwave Integrated Circuit
MMIC	Monolithic Microwave Integrated Circuit
NCO	Numerically Controlled Oscillator
NRE	Non-Recoverable Engineering costs
OCXO	Oven-Controlled Crystal Oscillator
PCB	Printed Circuit Board
PLL	Phase Locked Loop
ROM	Read Only Memory
SATCOM	Satellite Communications
SDLS	Satellite Data Links Standards
SOW	Statement of Work
TCXO	Temperature-Compensated Crystal Oscillator
VCO	Voltage Controlled Oscillator

EXECUTIVE SUMMARY

Fast-hopping frequency synthesizers suitable for space based applications are required to meet the demands of modern spread spectrum EHF communications. COM DEV was commissioned to conduct a comprehensive investigation into potential payload frequency-hopping synthesizer solutions. This report is the end product of this study.

The primary objective was to conduct, document, and submit a specification sensitivity analysis for the development of a payload frequency-hopping synthesizer. In compliance with the Statement of Work (SOW), this objective was achieved by the following three major tasks:

1) A literature review resulting in a recommendation of three potential frequency-hopping synthesizer approaches for further analysis.

2) Comparison of the three approaches on the basis of electrical, mechanical, and economic criteria, resulting in a recommended selection of the most favourable approach.

3) A detailed study on the selected approach addressing the viability of the design, the impact to the system of non-achievable specifications, and on the sensitivity of the design to specification.

Figure A shows the implementation of the final selected synthesizer design.

The proposed synthesizer uses an optimum combination of Direct Digital Synthesis (DDS) and Direct Analogue Synthesis (DAS) technology. A state-of-the-art high speed DDS is used to generate a baseband signal. A 32-bit digital input controls the frequency output of the DDS, which can be set anywhere between 50 MHz and 300 MHz with a resolution of 0.23 Hz. The required bandwidth and output frequency is produced by using DAS techniques (frequency mixing and multiplying). An Upconverter uses a combination of frequency multipliers and mixers to expand the DDS bandwidth and translate its output to the required 20.2 GHz to 21.2 GHz frequency range.

A detailed analysis of the preferred synthesizer approach revealed that it is viable to design and build a payload frequency-hopping synthesizer which will meet all of the given requirements. However, the synthesizer will not currently meet the required spurious and frequency accuracy due to current component technology limitations. The result will be a degradation in the system dynamic range and noise figure, which will necessitate a reduction in user traffic and data rates. Performance improvements in the spurious levels and the frequency accuracy are feasible based on projected component technology performance.

The results of the specification sensitivity analysis indicated that only a few of the specifications are highly sensitive to each other. These include the following:

1. *Centre frequency* is sensitive to the *phase noise* specification.
2. *Bandwidth* is sensitive to the *spurious* specification.
3. *Frequency accuracy* is sensitive to the *reference stability*.
4. *Spurious* levels are sensitive to the *bandwidth* requirements.
5. *Phase noise* is sensitive to the *reference phase noise* at offset frequencies less than 100 kHz.
6. *Reference phase noise* is sensitive to the output *phase noise* requirements at offset frequencies less than 100 kHz.

The sensitivity analysis is valid only with regard to the selected synthesizer approach. Other synthesizers may or may not exhibit the same sensitivity characteristics.

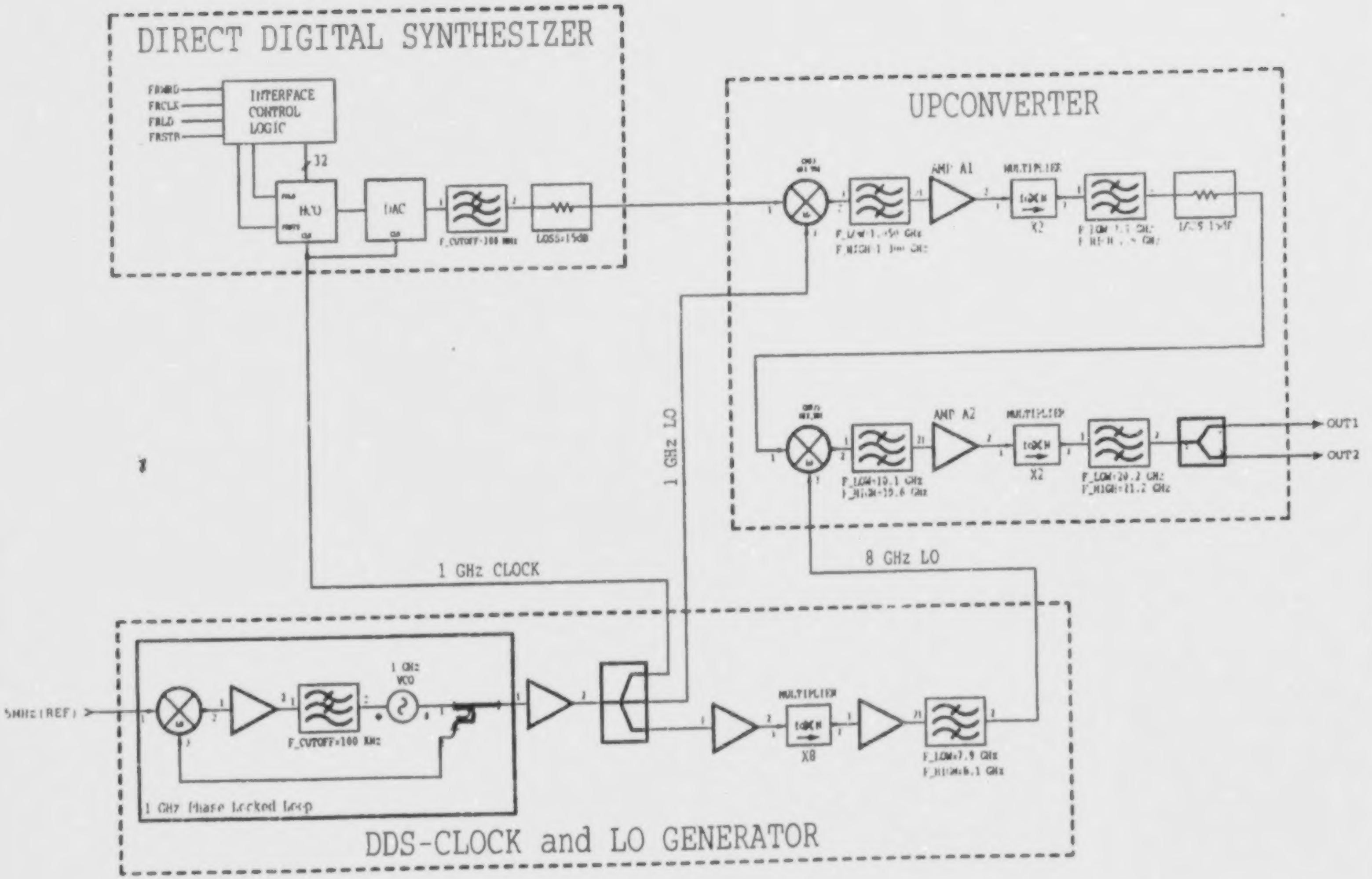
DIRECT DIGITAL SYNTHESIZER
FRWRD
FRCLK
FRLD
FRSTR
INTERFACE CONTROL LOGIC
32
NCO
DAC
F_CUTOFF=100 MHz
LOSS=15dB
UPCONVERTER
AMP A1
MULTIPLIER
X2
AMP A2
MULTIPLIER
X2
F_LOW=10.1 GHz
F_HIGH=10.6 GHz
F_LOW=20.2 GHz
F_HIGH=21.2 GHz
OUT1
OUT2
1 GHz LO
8 GHz LO
1 GHz CLOCK
5MHz(REF)
1 GHz VCO
F_CUTOFF=100 KHz
1 GHz Phase Locked Loop
MULTIPLIER
X8
F_LOW=7.9 GHz
F_HIGH=8.1 GHz
DDS-CLOCK and LO GENERATOR

Figure A: Detailed Block Diagram of the Proposed Synthesizer

COM DEV recommends the design, build, and test of a breadboard synthesizer using the approach identified in this study. The implementation described in this report represents an advancement over currently available space-qualified frequency-hopping EHF sources. Demonstrating the capability to build the synthesizer for space-based applications will help delineate Canada as a leader in EHF SATCOM spacecraft technology. In addition, the breadboard build would serve the following critical purposes:

1. The verification of electrical performance and mechanical characteristics.
2. Reduction of the risk involved with the use of advanced DDS technology.
3. The identification and development of critical assembly processes.

1.0 INTRODUCTION

Fast-hopping frequency synthesizers suitable for space based applications are required to meet the demands of modern spread spectrum EHF communications. COM DEV was commissioned to conduct a comprehensive investigation into potential payload frequency-hopping synthesizer solutions. This report is the end product of this study.

The primary objective was to conduct, document, and submit a specification sensitivity analysis for the development of a payload frequency-hopping synthesizer. In particular, the viability of implementing a synthesizer with the target specifications given in Table 1 was investigated. An impact and sensitivity assessment of changes to individual specifications on all other requirements was performed. In compliance with the Statement of Work (SOW) these objectives were achieved by the following three major tasks:

I. Task 1: A literature review of relevant articles on the analysis and design of frequency-hopping synthesizers was conducted. Direct Digital Synthesis (DDS), Direct Analog Synthesis (DAS), Phase-Locked Loop (PLL), and hybrid approaches to frequency synthesis were included in the review. Based on this research, COM DEV recommended to the Design Authority (DA) three potential frequency-hopping synthesizer solutions for further analysis, as detailed in Task 2 below.

II. Task 2: Upon approval by the DA, the three approaches proposed in Task 1 were compared in terms of the following parameters:

   (1) signal bandwidth
   (2) frequency resolution
   (3) frequency accuracy
   (4) settling characteristics for phase and frequency
   (5) spurious performance
   (6) phase noise
   (7) required reference stability and phase noise
   (8) size
   (9) weight
   (10) power consumption
   (11) cost

The most favourable of the three suggested frequency-hopping synthesizer approaches was recommended to the DA for a detailed study, as described in Task 3 below.

III. Task 3: Upon approval by the DA of the frequency-hopping synthesizer recommended in Task 2, the viability of implementing a design which satisfies the target specifications of Table 1 was determined. In the event that the specifications in Table 1 could not be met by the selected approach, an analysis was performed on the restrictions which the frequency synthesizer design places on the overall system design and compatibility with the Satellite Datalinks Standard (SDLS) waveform. In addition, a specification sensitivity analysis was performed. This was accomplished by substantially changing the individual specifications given in Table 1 and determining as quantitatively as possible the subsequent impact on each of the other specifications.

Table 1: Synthesizer Target Specifications

Serial	Parameter	Specification
1	Output Frequency	2 outputs @ 20.2 - 21.2 GHz
2	Frequency Resolution	≤ 200 Hz
3	Frequency Accuracy	± 100 Hz
4	Settling Characteristics (0.9 µs after frequency change)	≤ 1 kHz of target value ≤ 15° of target value within 10% of target amplitude
5	Spurious Performance	≤ -35 dBc
6	Phase Noise	≤ -66 dBc/Hz @ 1 kHz ≤ -108 dBc/Hz @ 1 MHz ≤ -118 dBc/Hz @ 1 GHz
7	Reference Stability and Phase Noise (5 MHz reference)	10^{-10} aging/day -130 dBc/Hz @ 10 Hz -148 dBc/Hz @ 1 kHz
8	Size	10^{-3} m^3
9	Weight	1.8 kg
10	Power Consumption	15 W

2.0 APPLICABLE DOCUMENTS

MIL-STD-1582C, "Satellite Data Links Standards (SDLS): Uplinks and Downlinks"

FASSET System Specification (Rev. 2. CN1, 7 Jan 92)

Statement of Work (SOW) entitled EHF SATCOM Payload Frequency Synthesizer Study, DREO 2790-1 (ED), 18 Jan 1993

Satellite Communications Engineering and Technical Research Support (Standing Offer), Contract #13SV.W8477-1-CC09

TNO/SKN/5085/001: Task 1 of the EHF SATCOM Payload Frequency Synthesizer Study

TNO/SKN/5085/002: Task 2 of the EHF SATCOM Payload Frequency Synthesizer Study

3.0 ASSUMPTIONS

Assumptions are invariably always required when conducting a study on a new product. Assumptions set the background upon which analysis, estimation, and comparison is performed. It is important that the assumptions are clearly stated, such that the pretence upon which certain conclusions and analytical results were derived are clearly understood. The major assumptions made in conducting this study are summarized here as follows:

- The synthesizer will require the following three internal power supplies, +7.5 V, +5 V, and -5.2 V. It is assumed that the spacecraft switching supplies will provide +8.0 V, +5.5 V, and -5.7 V, to the synthesizer. The additional regulation to the required voltage levels will be provided by the synthesizer.
- To minimize the required control lines, connector size, and subsequently the overall size of the synthesizer, a serial rather than a parallel frequency control interface was assumed.
- The use of radiation hardened CMOS was presumed to be acceptable. This minimized the required power consumption for the required interface logic.
- A mission life of 5 years was assumed.
- Phase noise performance is assumed to be 10 dB worse than calculations based on ideal equations.
- A qualification temperature range of -25 to +70 degrees Celsius, which is consistent with the flight requirements, was presumed.
- Phase noise is the primary concern of a synthesizer. Thermal noise effects on phase noise close to the carrier will be negligible. Adequate filtering will be provided to minimize effects on phase noise far away from the carrier (i.e. at offset frequencies > 500 MHz).
- An output power level of better than 3 dBm at both outputs will be required. In addition, flatness is assumed not critical, as well as temperature induced variations.

- Cost Analysis:
    - Based on cost to prototype only one synthesizer
    - Costs do not include qualification
    - Cost estimates are relative and not absolute
    - Cost estimates based on NRE requirements only
- No circuit redundancy will be required within the synthesizer to meet the required reliability criteria.

4.0 SUMMARY OF TASK 1 AND TASK 2 RESULTS

The results, findings, recommendations and/or conclusions of Tasks 1 and 2 were previously reported in the following two documents:

TNO/SKN/5085/001	TASK 1 of the EHF SATCOM PAYLOAD FREQUENCY SYNTHESIZER STUDY
TNO/SKN/5085/002	TASK 2 of the EHF SATCOM PAYLOAD FREQUENCY SYNTHESIZER STUDY

Copies of these documents are attached for convenience as Appendix A and Appendix B.

The references listed in the Task 1 report is only partially complete. A more complete bibliography is given in this report. In addition, a synopsis of relevant articles can be found in Appendix C.

The Task 1 report actually suggested four rather than three synthesizer options. However, only three of these options were selected for Task 2. In addition, the three selected synthesizer approaches were modified in the Task 2 report to provide improved performance. These modified options are repeated here (Figures 1, 2 and 3) for easier reference.

The conclusion of Task 2 was to recommend Option 1 (see Figure 1) for further study in Task 3, because it exhibits the best electrical and mechanical characteristics, least cost, and least risk. For a more extensive comparison see the Task 2 report (Appendix B).

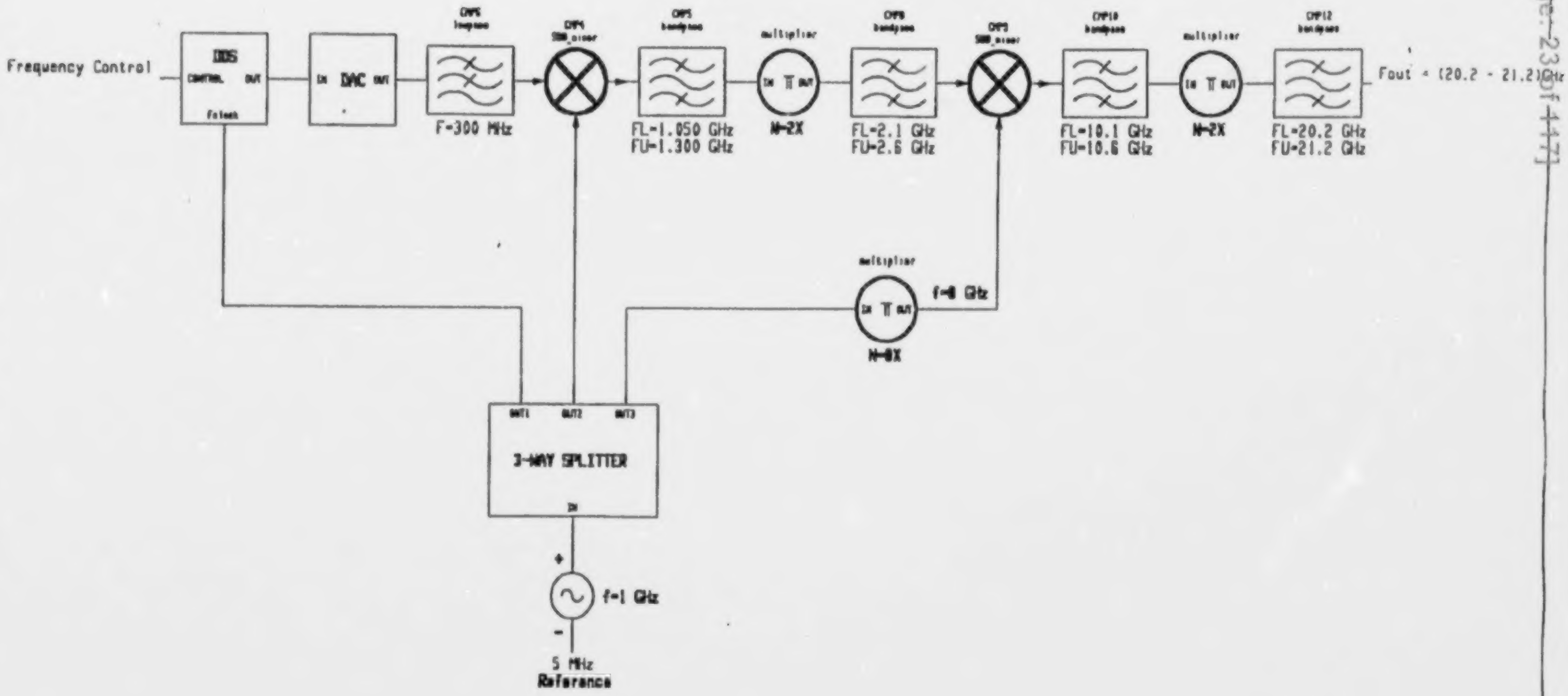
Frequency Control
DDS
CONTROL
OUT
Fclock
IN
DAC
OUT
lowpass
F=300 MHz
SSB_mixer
bandpass
FL=1.050 GHz
FU=1.300 GHz
multiplier
IN
OUT
N=2X
bandpass
FL=2.1 GHz
FU=2.6 GHz
SSB_mixer
bandpass
FL=10.1 GHz
FU=10.6 GHz
multiplier
IN
OUT
N=2X
bandpass
FL=20.2 GHz
FU=21.2 GHz
Fout = (20.2 - 21.2)GHz
multiplier
IN
OUT
f=8 GHz
N=8X
OUT1
OUT2
OUT3
3-WAY SPLITTER
IN
+
f=1 GHz
-
5 MHz
Reference

Figure 1: Option 1 DDS/Direct Analogue Frequency Synthesizer

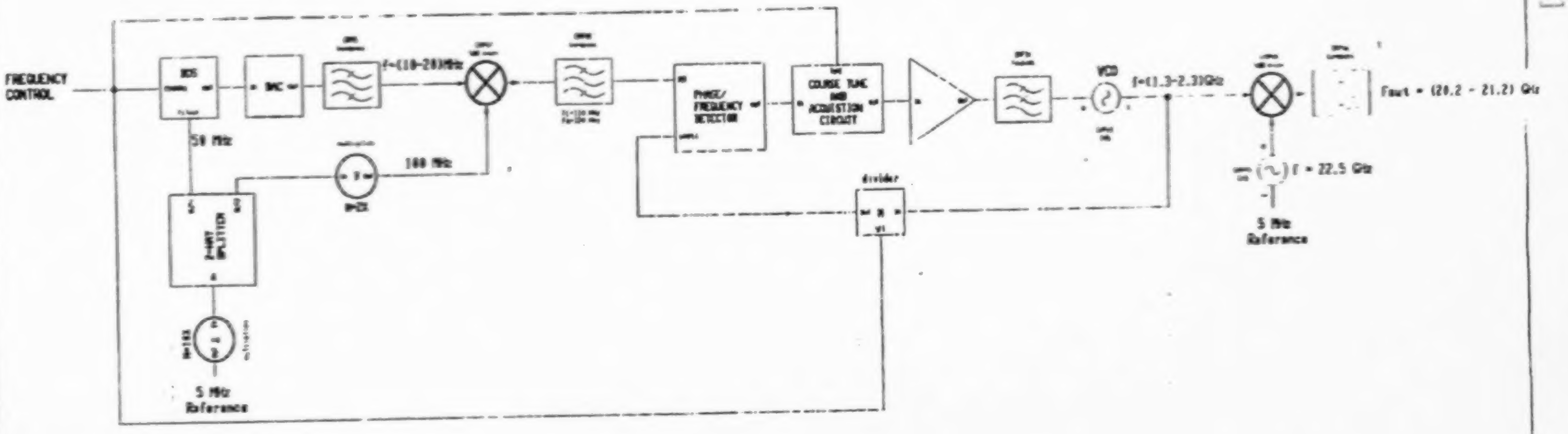
FREQUENCY CONTROL
DDS
DAC
f=(10-20)MHz
50 MHz
100 MHz
2-WAY SPLITTER
5 MHz Reference
PHASE/ FREQUENCY DETECTOR
COURSE TUNE AND ACQUISITION CIRCUIT
VCO
f=(1.3-2.3)GHz
divider
Fout = (20.2 - 21.2) GHz
f = 22.5 GHz
5 MHz Reference

Figure 2: Option 2 DDS Driven PLL Frequency Synthesizer

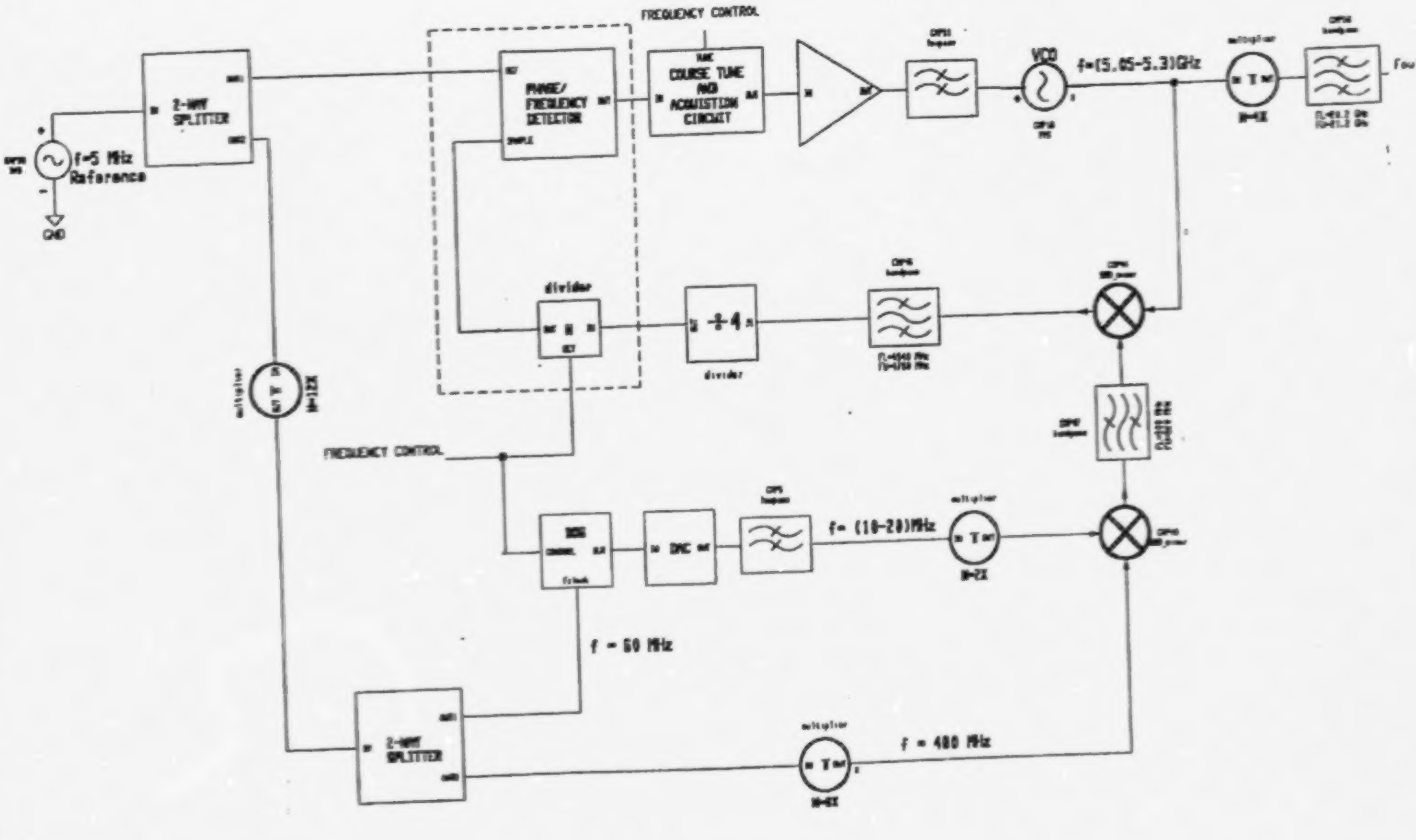
f=5 MHz
Reference
GND
2-WAY
SPLITTER
PHASE/
FREQUENCY
DETECTOR
FREQUENCY CONTROL
COURSE TUNE
AND
ACQUISITION
CIRCUIT
VCO
f=(5.05-5.3)GHz
multiplier
Fout = (20.2 - 21.
divider
÷4
divider
multiplier
FREQUENCY CONTROL
DDS
DAC
f= (10-20)MHz
multiplier
f = 60 MHz
2-WAY
SPLITTER
multiplier
f = 400 MHz

Figure 3: Option 3 PLL with DDS Frequency Offset

5.0 DETAILED DESCRIPTION OF THE SYNTHESIZER

The proposed synthesizer uses an optimum combination of Direct Digital Synthesis (DDS) and Direct Analogue Synthesis (DAS) technology. A detailed block diagram of the selected synthesizer approach is given in Figure 4. A state-of-the-art high-speed DDS is used to generate a baseband signal. A 32-bit digital input controls the frequency output of the DDS, which can be set anywhere between 50 MHz and 300 MHz with a resolution of 0.23 Hz. The required bandwidth and output frequency is produced by using DAS techniques (frequency mixing and multiplying). An Upconverter uses a combination of frequency multipliers and mixers to expand the DDS bandwidth and translate its output to the required 20.2 GHz to 21.2 GHz frequency range.

The synthesizer consists of three major functional groups: the DDS, the DDS-Clock and LO Generator, and the Upconverter. These are explained in more detail in the following sections.

5.0.1 The Direct Digital Synthesizer

At the heart of the synthesizer is a high speed DDS which is operated at a clock frequency of 1 GHz. It consists of a 32-bit Numerically Controlled Oscillator (NCO), an eight-bit Digital to Analogue Converter (DAC), a lowpass filter (LPF), and some CMOS interface and control logic.

The NCO is a single chip device which outputs successive samples of an encoded sine waveform. A block diagram of a typical NCO is given in Figure 5. The NCO is simply a combination of a digital phase accumulator and a Read Only Memory (ROM) which is encoded with sequential samples of a sine waveform. At each clock transition, the phase accumulator is incremented by the number stored in the *Delta-Phase Register*. The contents of the *Delta-Phase Register* is set by latching the desired 32-bit frequency control word into it. The number stored in the *Phase Accumulator* represents the current phase of the required sinusoidal waveform. The 20 most significant bits of the *Phase Accumulator* address the ROM lookup table, which outputs an 8-bit word that corresponds to the amplitude of the sine wave at the selected phase. The resulting output of the NCO is a series of 8-bit digital samples of a sine wave, spaced at intervals corresponding to the DDS clock period.

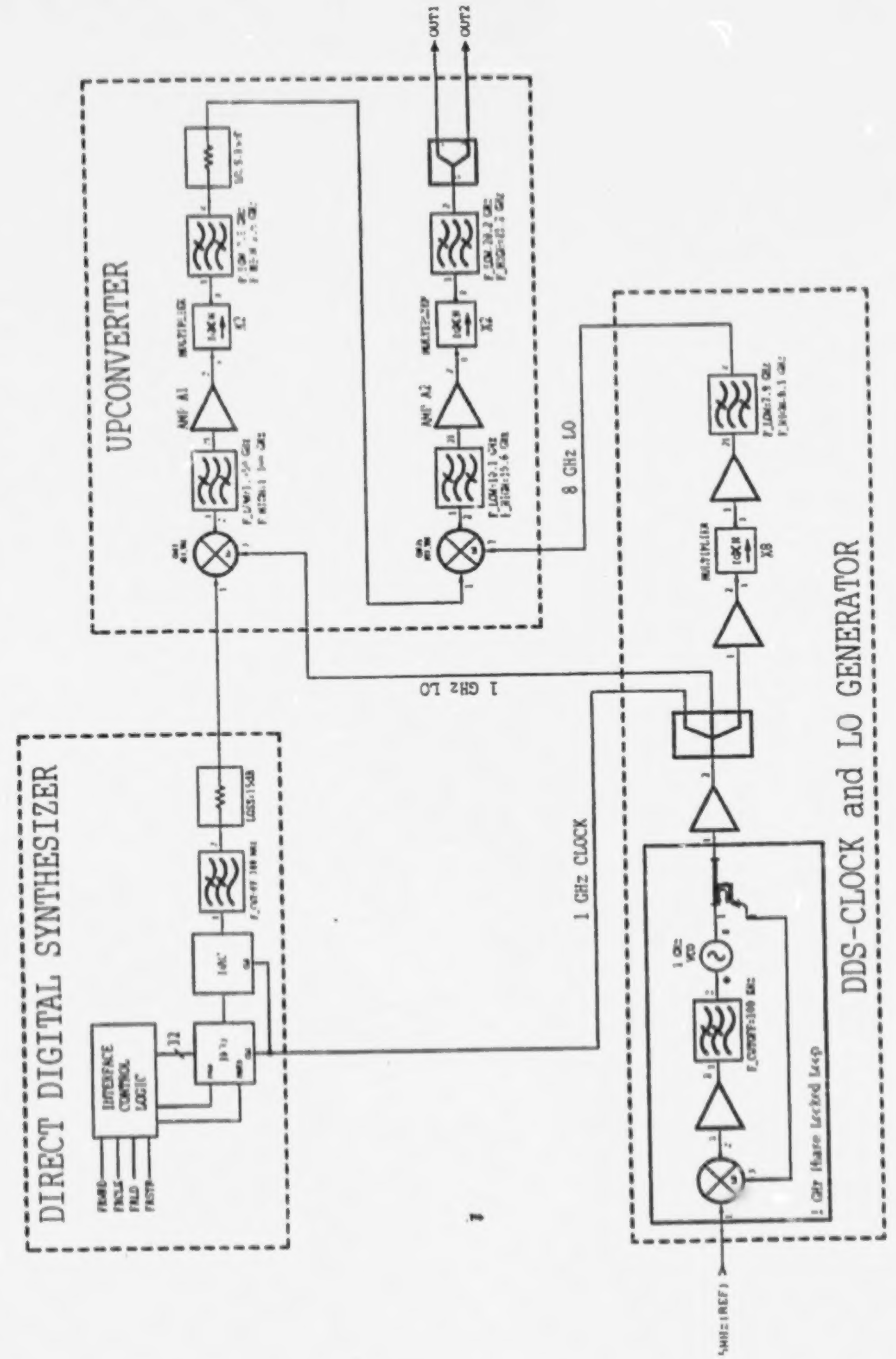
DIRECT DIGITAL SYNTHESIZER
INTERFACE CONTROL LOGIC
32
DAC
LOSS:15dB
UPCONVERTER
AMP A1
AMP A2
MULTIPLIER
X2
OUT1
OUT2
1 GHz LO
8 GHz LO
1 GHz CLOCK
DDS-CLOCK and LO GENERATOR
MULTIPLIER
X8
1 GHz VCO
1 GHz Phase Locked Loop
5MHz (REF)

Figure 4: Detailed Block Diagram of the Synthesizer

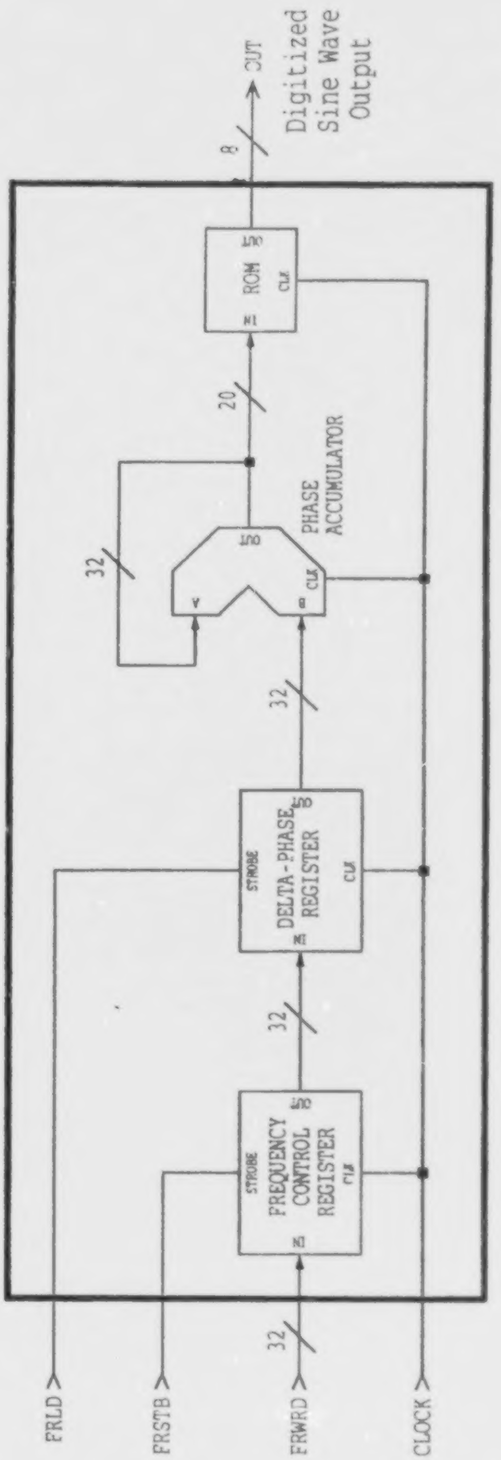
OUT
8
Digitized Sine Wave Output
ROM
IN
OUT
CLK
20
PHASE ACCUMULATOR
32
A
B
OUT
CLK
32
DELTA-PHASE REGISTER
STROBE
IN
OUT
CLK
32
FREQUENCY CONTROL REGISTER
STROBE
IN
OUT
CLK
32
FRLD
FRSTB
FRWRD
CLOCK

Figure 5: Block Diagram of a Typical NCO

The output of the NCO is used to drive a high-speed Digital to Analogue Converter (DAC). The DAC converts the digital sine-wave generated by the NCO into the required analogue sine-wave, at the frequency selected by the *frequency control word* (FRWRD).

Setting the DDS output frequency is accomplished via the Interface and Control Logic. The required 32-bit *frequency control word* (FRWRD) is input via a two-wire differential line using a serial-synchronous protocol. FRCLK (Frequency Control Word Data Clock) establishes the required synchronisity to effectively stream-in the frequency control word. Two additional signals, FRSTB (Frequency Strobe) and FRLD (Frequency Load), are required to complete the control of the synthesizer. FRSTB is used to latch the FRWRD into the *Frequency Control Register* of the NCO, once the serial transfer of all 32 bits of the control word is complete. A frequency change is not commenced until a FRLD command is received. The FRLD command loads the current contents of the *Frequency Control Register* into the *Delta-Phase Register*, which is subsequently added to the stored value of the *Phase Accumulator*. This results in the required output frequency change while maintaining complete phase coherency. Phase coherency is maintained, because the new contents of the *Delta-Phase Register*, which corresponds to the new desired output frequency, is added directly to the current value of the *Phase Accumulator*.

The DDS is capable of providing output frequencies from 0 to 400 MHz in 0.23 Hz steps. However, to facilitate image rejection in the upconverter the minimum output of the DDS is restricted to 50 MHz. This establishes a guard band of 50 MHz, which is large enough to allow adequate image rejection at the first-stage of upconversion.

The maximum output of the DDS is restricted to 300 MHz rather than its maximum capability of 400 MHz. This was done in order to allow some margin of safety in the design. Although present DDS technology can be clocked at 1 GHz, they usually can only accomplish this at a reduced temperature environment. Setting the maximum output frequency at 300 MHz will allow the clock frequency to be reduced, if necessary, to at least 800 MHz. A clock frequency of 800 MHz will usually allow operation over the entire military temperature range (-55°C to + 125°C). Unfortunately, the change in clock frequency will require additional real estate and dc power consumption. However, sufficient margin exists in the volume, mass and power consumption compared to the specifications to accommodate the required modifications.

5.0.2 The DDS-Clock and Local Oscillator Generator

The DDS-Clock and LO Generator consists of a 1 GHz PLL, a 3-way power divider, and a times-eight frequency multiplier.

The PLL locks a 1 GHz VCO to the 5 MHz input reference frequency. The 1 GHz PLL output is subsequently amplified to a level of about 16 dBm. A three-way power splitter provides three outputs, at 1 GHz, with a nominal output power level of 10 dBm. One of these outputs is used as the DDS clock, and another as the local oscillator for the first upconversion stage. The third output is amplified and multiplied to 8 GHz, in order to provide the required local oscillator for the second upconversion stage.

5.0.3 The Upconverter

The function of the upconverter is two-fold; it translates the DDS signal to the required output frequency and performs bandwidth expansion. Two stages of frequency upconversion and frequency-doubling are used.

The first upconversion stage translates the DDS signal to a frequency range of 1.050 GHz to 1.300 GHz. The output of the DDS is attenuated to a level below -15 dBm prior to the mixer. This guarantees that any in-band mixer spurious will be lower than the inherent -42 dBc spurious of the DDS output.

The first-stage upconverter output is translated to the frequency range of 2.1 GHz to 2.6 GHz by the first-stage frequency doubler. Amplifier "A1" amplifies the upconverter output and drives the frequency-doubler with about 10 dBm of power. In addition to doubling the input frequency, the frequency-doubler also doubles the available signal bandwidth from 250 MHz to 500 MHz.

Translation of the first-stage doubler output to a range of 10.1 GHz to 10.6 GHz is accomplished by the second-stage upconverter. To achieve the required -35 dBc output spurious specification, the second-stage upconverter intermodulation product levels must be lower than -41 dBc. To achieve this, the input signal applied to the mixer is attenuated to a level below -15 dBm. This guarantees that the levels of any in-band mixer intermodulation products will be sufficiently low.

Amplifier "A2" amplifies the second-stage upconverter output to a level of about 20 dBm. The amplifier drives the second-stage frequency doubler which provides the required output signal range of 20.2 GHz to 21.2 GHz.

This doubler expands the 500 MHz bandwidth, at its input, to the required 1 GHz signal bandwidth.

A two-way power-divider provides the two required outputs. The output signal level will be approximately 5 dBm at each of the outputs.

5.1 Predicted Performance of the Synthesizer

The predicted performance of the synthesizer is summarized in Table 2. A detailed description of each parameter is given in the following sections.

5.1.1 Signal Bandwidth

The selected DDS approach will provide a synthesized sine-wave with a frequency between 50 MHz and 300 MHz. This translates to a usable DDS bandwidth of 250 MHz. The two frequency-doublers, incorporated in the Upconverter, provide the required bandwidth expansion to 1 GHz.

5.1.2 Frequency Resolution

The frequency resolution of the synthesizer is simply four times the frequency step-size of the DDS. The factor of four degradation in the output resolution is a byproduct of the required bandwidth expansion performed by the frequency-doublers within the Upconverter. The DDS step size is given by,

$$\Delta f_{dds} = \frac{f_{clk}}{2^N}$$

where,

f_{clk} = the DDS clock frequency
N = the number of bits in the *frequency control word*.

With a 32-bit *frequency control word* and a DDS clock frequency of 1 GHz, the frequency step size of the DDS will be 0.23 Hz. The resulting overall synthesizer resolution will be four times this amount, which is 0.92 Hz. This differs from the value originally reported in the TASK 2 report because a 31-bit frequency control word was used in that analysis.

The specification requires a frequency resolution of only 200 Hz. The predicted resolution of 0.92 Hz is well within this requirement.

Table 2: Predicted Performance of the Synthesizer

Serial	Parameter	Specification	Performance
1	Signal Bandwidth	20.2 - 21.2 GHz	20.2 - 21.2 GHz
2	Frequency Resolution	<= 200 Hz	0.92 Hz
3	Frequency Accuracy	100 Hz	100 Hz
4	Settling Time <= 1KHz of target value <= 15 degrees of target value within 10% of target amplitude	<= 900 nSec	<= 100 nSec
5	Spurious Performance	<= -35 dBc	<= -30 dBc
6	Phase Noise	<= -66 dBc/Hz @ 1 kHz <= -108 dBc/Hz @ 1 MHz <= -118 dBc/Hz @ 1GHz	<= -69 dBc/Hz @ 1 kHz <= -111 dBc/Hz @ 1 MHz <= -160 dBc/Hz @ 1GHz
7	Reference Stability and Phase Noise (5 MHz Reference)	1E-10 aging/day -130 dBc/Hz @ 10 Hz -148 dBc/Hz @ 1 kHz	3E-12 aging/day -130 dBc/Hz @ 10 Hz -148 dBc/Hz @ 1 kHz
8	Size	1000 cc	625 cc
9	Weight	1.8 Kg	1.4 Kg
10	Power Consumption	15 W	12.75 W

5.1.3 Frequency Accuracy

The frequency accuracy of the synthesizer stipulates how accurately its output can be set to a desired frequency. The required accuracy is 100 Hz.

Irrespective of the synthesizer architecture the output frequency must always be phase locked to the reference frequency. The locking process causes the output frequency to track the reference frequency. A small change in the reference frequency is translated to a proportionately larger shift in the output frequency. The resulting frequency deviation at the synthesizer output is,

$$\Delta f_{out}=\Delta f_{ref}(\frac{f_{out}}{f_{ref}})$$

where,

f_{out} = the desired output frequency,
f_{ref} = the nominal reference frequency,
Δf_{ref} = the deviation of the reference frequency from nominal.

The worst case frequency deviation will occur at the maximum output frequency of 21.2 GHz. The specified stability of the 5 MHz reference frequency is 1E-10 aging/day. This will yield a worst case frequency drift of 2.12 Hz per day at the synthesizer output.

Assuming a mission life of 5 years, the resulting worst case frequency accuracy would be 3869 Hz. This does not meet the specified accuracy of 100 Hz. To remain within 100 Hz, worst case, the frequency reference would require a stability of at least 3E-12 aging/day, or for calibration to be performed at least once every 45 days.

5.1.4 Settling Characteristics

The frequency synthesizer will exhibit some latency between the time that a frequency load command is received and the moment that the output frequency changes. This latency is a result of the inherent propagation delay of the logic circuits within the DDS, and the group delay associated with the various RF components. However, with the exception of this propagation delay, the output frequency will appear to change instantaneously with minimal transients. This is a byproduct of the DDS generated waveform, which maintains phase coherence and hence, amplitude continuity, when the frequency is changed.

The synthesizer, however, will not have a perfectly flat amplitude response across its entire output frequency range. Sources of amplitude variation with frequency include, the amplitude droop of the DAC at the higher output frequencies, as well as the ripple associated with the various RF components. The result of this amplitude variation with frequency will be some minor amplitude transients when switching frequencies. Any amplitude ringing which does occur, will decay to an acceptable level within 10 time constants of the narrowest filter bandwidth within the signal path. Although the amplitude ringing can create some phase modulation within the amplifiers, mixers, and frequency multipliers, the degree to which this will occur will be negligible.

A frequency transition is commenced when the synthesizer receives a frequency load (FRLD) command. The DDS requires 25 clock cycles before its output changes frequency. With a 1 GHz clock, the DDS will switch frequencies in 25 nsecs. The combined group delay of the filters, amplifiers, mixers, and multipliers, will be less than 50 nsecs. The resulting net delay before the synthesizer output changes frequency will be 75 nsecs. As discussed, depending on the amplitude flatness of the synthesizer, some degree of amplitude transient oscillation will occur. The narrowest filter bandwidth in the synthesized signal path is 250 MHz, which means that it has a time constant of about 1.5 nsecs. The synthesizer output will settle to within 1% of the desired amplitude in 15 nsecs. The overall switching time, including propagation delay will be approximately 90 nsecs. This handily meets the required settling time of 900 nsecs.

5.1.5 Spurious Performance

If the selected synthesizer approach has an Achille's heal, it is the spurious noise content, estimated to be roughly -30 dBc. The primary source of the spurious signals is the DDS, which based on the best currently available DDS technology, will contain a worst-case spurious level of -42 dBc. The required four-times bandwidth expansion, provided by the frequency multipliers in the Upconverter, will further degrade the spurious levels by 12 dB to the predicted -30 dBc level. Unfortunately, this means that the -35 dBc requirement will not be met with the selected synthesizer approach.

The spectral purity of a DDS generated waveform is a function of many variables, including phase quantization, amplitude quantization, the ratio of clock frequency to output frequency, and the dynamic characteristics of the DAC. The best available high-speed NCO generates a sine function which has 8-bit amplitude quantization and 10-bit phase quantization. This results in spurious levels which are theoretically about -48 dBc.

Conversion of the digitized sine wave into the required analogue signal defines the practical limit to the achievable spur levels. The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates. In addition, glitch energy produced by timing inaccuracies also contribute significantly to the spurious content of the DAC output. The best available high-speed DAC exhibits a spurious output level of -42 dBc.

The required synthesized signal bandwidth requires that almost the complete range of the DDS output frequency be used. This means that at the lower DDS frequencies some intermodulation products, generated by the upconversion process, will fall within the required output signal band. To circumvent this problem, the synthesized signal is attenuated to below -15 dBm prior to each of the two mixers. This guarantees that any in-band mixer generated spurious levels will be better than -60 dBc. In addition, out-of-band mixer products, including the "image" response, are reduced by the various bandpass filters.

5.1.6 Phase Noise

A first order approximation of the synthesizer's output phase noise is plotted in Figure 6 as a function of offset frequency from the carrier. The phase noise results from a number of different contributing noise sources. The main sources of phase noise in the synthesizer are the DDS and the two local oscillators.

The 1 GHz local oscillator is derived from a VCO which is phase locked to the externally provided 5 MHz reference. The fundamental property of a PLL is that, at offset frequencies within the loop bandwidth, the output phase noise will be the reference phase noise degraded by the division factor of the PLL. The amount of reference oscillator phase noise degradation will be 20log(N), where N is the ratio of the output frequency to the reference frequency. In this case, N = 200, which yields a 46 dB degradation in the reference noise. At offset frequencies above the loop bandwidth, the output phase noise will be equal to the VCO phase noise.

The 8 GHz local oscillator is generated from the 1 GHz local oscillator by using an 8-times frequency multiplier. When a signal is frequency multiplied its phase noise is degraded by 20log(N), where N is the multiplication factor. The resulting phase noise of the 8 GHz local oscillator will be simply that of the 1 GHz local oscillator degraded by 18 dB (i.e. 20log(8)) at all offset frequencies within the post-multiplier filter bandwidth. Outside this bandwidth the filter rejection will improve the phase noise.

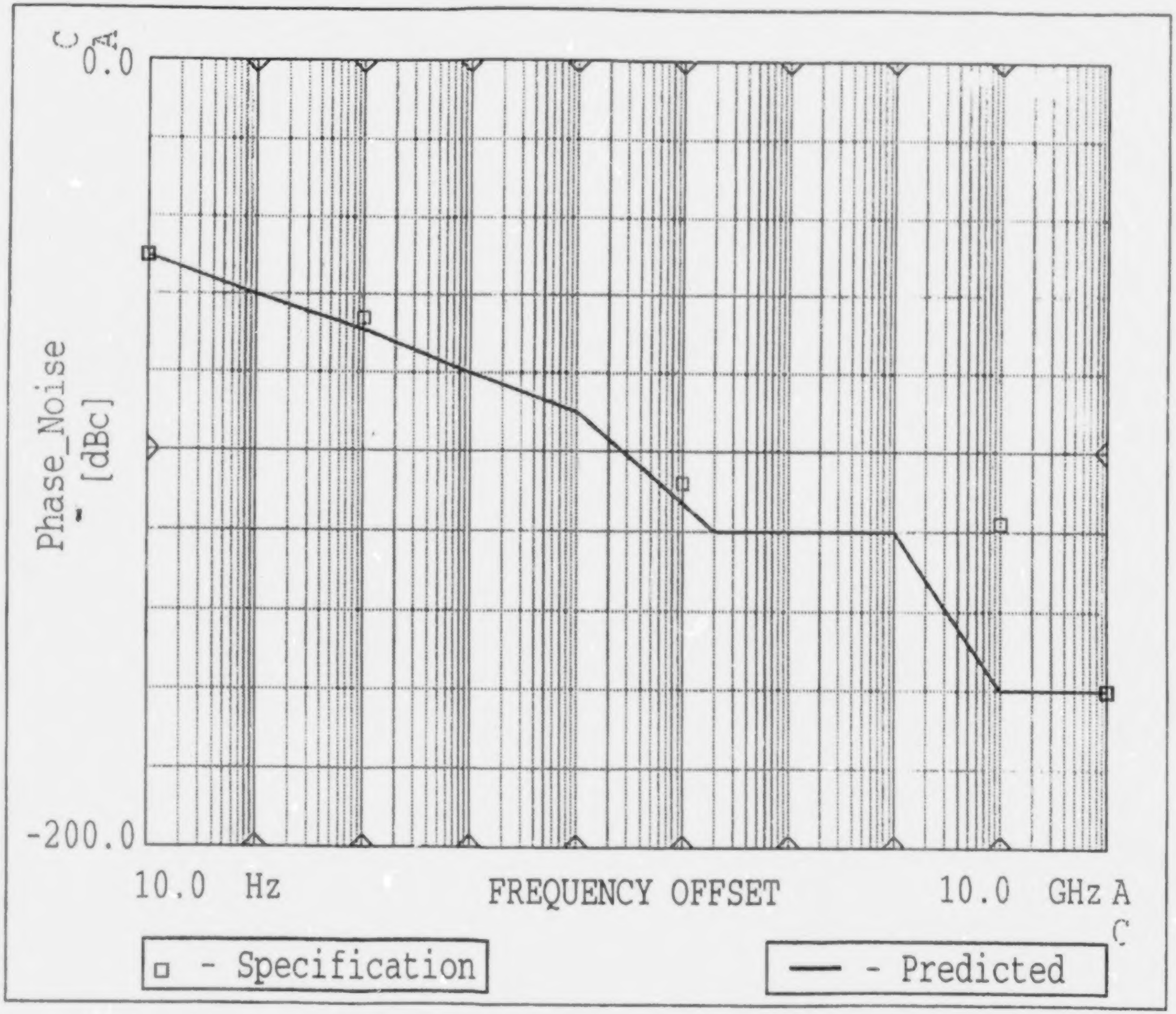

Figure 6: Predicted Phase Noise of the Synthesizer

At offset frequencies below approximately 1 MHz, the phase noise of the DDS output is the phase noise of the clock improved by 20log(X), where X is the ratio between the clock frequency and the output frequency. The worst-case phase noise of the DDS output will occur at its maximum output frequency. In this synthesizer implementation the maximum DDS output frequency is 300 MHz. The resulting phase noise will be the phase noise of the 1 GHz local oscillator improved by approximately 10 dB (i.e. 20log(1GHz/300MHz). However at offset frequencies above 1 MHz, the phase noise will be limited to the DDS noise floor. The noise floor of the DDS will be significantly higher than that of the 1 GHz local oscillator. The GaAs based digital circuits, which are used in the DDS, will limit the noise floor to approximately -140 dBm. Assuming a minimum DDS output power of 0 dBm, results in a worst case phase noise floor of -140 dBc.

At offset frequencies up to approximately 1 MHz, the synthesizer's phase noise is determined by the 8 GHz local oscillator noise, degraded 6 dB by the final-stage frequency doubler. Between offset frequencies of approximately 1 MHz and 100 MHz the phase noise is limited by the unconverted DDS noise floor, which is degraded 12 dB by the two frequency doublers. Beyond the 100 MHz offset frequency, the phase noise is rapidly attenuated by the filters within the synthesized signal path to a level determined by the thermal noise floor. An additional 10 dB degradation was added at all offset frequencies to account for the non-ideality of the various components. The resulting phase noise at the specified offset frequencies of 1 kHz, 1 MHz, and 1 GHz are -69 dBc, -111 dBc, and -160 dBc, respectively. These meet the requirements, which are -66 dBc, -111 dBc ,and -118 dBc, at the respective offset frequencies.

The phase noise at the specified offset frequencies of 1 kHz, 1 MHz, and 1 GHz are determined by three separate sources. At the 1 kHz and 1 MHz offsets, the phase noise is determined by the 8 GHz local oscillator. This oscillator's phase noise is, in turn, determined by the reference oscillator at 1 kHz, but by the VCO phase noise at the 1 MHz offset. At an offset frequency of 1 GHz the limitation is the thermal noise floor.

5.1.7 Required Reference Stability and Phase Noise

The selected frequency synthesizer approach will meet the required phase noise with the specified reference phase noise levels. The reference phase noise determines the phase noise of the output signal at frequency offsets less than 100 kHz. This corresponds to the bandwidth of the PLL. Beyond the 100 KHz offset, the reference oscillator has little or no effect on phase noise.

The required 100 Hz frequency accuracy cannot be achieved by any implementation with the specified reference frequency stability. Assuming a 5 year mission life, the required stability of the 5 MHz reference, to maintain a frequency accuracy of 100 Hz, is approximately 3E-12 aging/day. This level of stability can only be provided by a Cesium or Rubidium atomic standard. An alternative to these atomic standards is to calibrate the synthesizer or reference oscillator at regular intervals. With the specified stability of 1E-10 aging/day, calibration would be required at least once every 45 days.

5.1.8 Size and Mass

A size and mass estimate was developed by dividing the synthesizer into the various sub-modules. The key components required by each of these modules were then identified. Component sizes were determined from various catalogues and or similarity to previous COM DEV designs. This data was then used to perform a preliminary layout for each of the modules. These module layouts were then used to piece together an approximate layout of the overall synthesizer. The size and mass of the various modules were added together to provide an estimate of the overall synthesizer mass and size. The predicted size of the synthesizer is approximately 625 cc, with a corresponding mass of 1.4 kg. This meets the specified mass and size of 1.8 kg and 1000 cc, with significant design margin. However, this deviates from the original size and mass estimates of 545 cc. and 1.25 kg, given in the Task 2 report. The increases arise from improved DC-power regulation and filtering over that assumed in the Task 2 report.

5.1.9 Power Consumption

A power consumption estimate for the selected synthesizer approach was arrived at by generating an approximate schematic representation for the DDS, the Upconverter, the DDS Clock and Local Oscillator Generator, and the Interface and Control Logic. Parts lists for each of the modules were then generated. Standard catalogue items or internal COM DEV products were used for all of the parts. The specified power consumption of each component was then determined from the manufacture's specifications and totalled to yield an estimate of the synthesizer power consumption. The resulting predicted power consumption for the synthesizer is approximately 12.75 watts. This meets the requirement of 15 watts with sufficient design margin. However, this is slightly greater than the power estimate originally reported in the Task 2 report. The additional power consumption is necessary to accommodate the regulation and filtering of the various power rails. Power estimates of all three synthesizer options in the Task 2 report, did not include adequate provisions for power supply filtering and regulation.

5.2 Envisioned Synthesizer Build

While an exact determination of the synthesizer build is not possible without more detailed specifications and a comprehensive design effort, a conceptual description can be given.

The frequency-hopping synthesizer will be contained in an aluminum housing approximately 7.5 x 6.75 x 0.75 inches. This small size will be achieved by utilizing a combination of surface mount and chip and wire manufacturing technologies. In addition, an optimum blend of MIC (Microwave Integrated Circuit), MMIC (Monolithic Microwave Integrated Circuit), and standard PCB (Printed Circuit Board) technologies will be used. Internally, the housing will be divided into a number of smaller compartments, within which the various sub-modules will be inserted. The major sub-modules include the DDS, the DDS-Clock and Local Oscillator Generator, and the Upconverter.

For optimum performance and reliability it is envisioned that the DDS will be manufactured using unpackaged die for both the NCO and the DAC. In addition, the CMOS control logic will also utilize unpacked die. A multilayer substrate will provide the media for the various inter-chip connections. For optimum heat-sinking, the NCO and DAC will be mounted on metal pedestals attached directly to the housing floor.

The DDS-Clock and Local Oscillator Generator will be split into at least two separate compartments. One compartment will contain the 1 GHz PLL and the second the required 8 GHz local oscillator generation module. The 1 GHz PLL will consist of at least 1 PCB on which the baseband circuitry will be mounted. The VCO and RF-coupler will be manufactured on a separate MIC module. The 8 GHz local oscillator generation module will consist of about four or five MIC assembles which will be bolted to the bottom of the synthesizer housing.

The Upconverter will be built entirely with MIC technology. At least 10 separate MIC modules will be required to realize the various upconversion functions. Each of these MIC modules will be separately assembled and tested before being bolted into the synthesizer housing. Standard off-the-shelf components will be used to keep cost to a minimum. These include surface mount mixers and amplifiers.

All RF interfaces will be either SMA or K-type connectors. DC and control interfaces will be provided via a number of solder-pin feedthroughs or by a multi-pin connector.

6.0 VIABILITY, SPECIFICATION NON-CONFORMANCE, AND SPECIFICATION SENSITIVITY

6.1 Viability of Implementing the Selected Approach

Implementing a frequency synthesizer which satisfies the requirements detailed in Table 1 is feasible with the selected approach. The majority of the required technology is well established and readily available. The synthesizer is simply a frequency upconverter which, for the most part, can be built using standard microwave components such as mixers, frequency multipliers, amplifiers, and filters. Their is nothing inherently difficult in designing and manufacturing these components. In addition, none of these components will require any extraordinary performance which is beyond the capabilities of current technology.

However, meeting the required output spurious signal levels is currently not possible with presently available DDS technology. The limiting factor on the spurious performance is the dynamic linearity of the DAC required to implement the high-speed DDS. The estimated spurious performance of -30 dBc is based on the use of TRIQUINT's TQ6122 8 bit, 1 GHz, DAC in tandem with STANFORD TELECOM's 2173 NCO. The TQ6122 is specified to provide a dynamic linearity which is typically better than -42 dBc. This is the best available performance from all currently available DACs. Improvement in the spurious performance is possible, as new DACs with better dynamic linearity are currently in development by various vendors.

A four company consortium consisting of SCITEQ, TRIQUINT, MOTOROLA, and SANDIA LABS, are jointly involved in the design of a 14-bit high-speed DAC. This product is projected to provide a dynamic linearity of better than -55 dBc, when clocked at 1 GHz. This would improve the spurious levels of the selected synthesizer to an impressive -43 dBc. TRIQUINT will eventually market this product as the TQ6140. Samples of this part are currently available from TRIQUINT. The TQ6140 should be available, on a commercial basis, sometime in the first quarter of 1994.

SCITEQ is also independently developing a fully monolithic DDS which incorporates an on chip 10-bit DAC. This device is expected to provide a spurious level better than -52 dBc at an 800 MHz clock rate. This product will be available on a sample basis in the fall of 1993. Incorporation of this new DDS into the synthesizer would result in a maximum spurious level of -40 dBc.

Initial indications from the above suppliers suggest that both the TQ6140 and SCITEQ's monolithic DDS can be provided to space quality levels by early 1995.

6.2 Specification Non-Conformance Impact Assessment

Two of the target specifications given in Table 1 cannot be met by the selected synthesizer approach. These are the spurious signal levels and the frequency accuracy.

Current technology limits the spurious performance of the synthesizer to -30 dBc which exceeds the requirements by 5 dB. This would reduce the signal to noise ratio and the dynamic range of the communications synthesizer, and result in increased error rates, as well as decreased user traffic. However, the spurious levels can be decreased to meet the requirements of -35 dBc (see section 6.1)

The frequency accuracy of the synthesizer is directly related to the stability of the externally provided reference oscillator (see section 5.1.3 for a detailed discussion). With the specified reference stability of 1e-10 aging/day the output would drift by about 3869 Hz over a 5 year period. This exceeds the required 100 Hz accuracy by an appreciable amount. The effect of this on the communications system is to decrease the signal to noise ratio. This occurs because the demodulation does not occur at the optimum point of the received signal. However, a frequency accuracy of 100 Hz can be maintained by calibrating at regular intervals. Calibration can be performed by either adjusting the reference oscillator at regular intervals, or by compensating the synthesizer by incorporating a frequency offset in the frequency control word.

6.3 Specification Sensitivity Analysis

A specification sensitivity analysis was performed. This was accomplished by substantially changing each of the individual specifications given in Table 1 and determining the subsequent impact to each of the other specifications. To accomplish this, the effect of the individual specification change on the other performance parameters of the synthesizer was determined first. The resulting performance for each of these synthesizer parameters were then compared to their governing specifications in order to determine their respective sensitivities. Sensitivities were classified into one of four levels These four levels of sensitivity are numbered from 0 to 3 and are defined as:

"0" - Not sensitive. No change in the synthesizer performance. No specification change is required.

"1" - Minor sensitivity. The synthesizer performance would exhibit an insignificant change with respect to the degree to which the original performance was in/out of specification.

"2" - Intermediate sensitivity. The synthesizer performance would exhibit a significant change with respect to the degree to which the original performance was in/out of specification. However, the change would be insufficient to cause a previously compliant condition to become non-compliant and vice-a-versa.

"3" - Major sensitivity. The synthesizer performance would exhibit a very significant change with respect to the degree to which the original performance was in/out of specification. The change would be sufficient to cause a previously compliant condition to become non-compliant and vice-a-versa.

Table 3 gives a summary of the specification sensitivities. This table indicates the amount by which each of the individual specifications was changed. The corresponding sensitivity of each of the other specifications to this change are classified according to the above criteria.

It is difficult to access exactly what constitutes a substantial change for each individual specification. The criteria used is specification dependant. In some instances the specification was changed by an amount that represents a reasonable range that could be required for various foreseeable applications. Other specifications were changed based on the magnitude of the margin that exists between the requirement and the predicted performance. Obviously, a specification that can be acheived with significant margin can be changed by a larger amount than a specification which is difficult to meet.

In the analysis only first order sensitivities were considered. A first order effect is one in which a change in specification "A" impacts specification "B" directly. A second order effect would be one in which a change in specification A causes a change in specification B which subsequently causes a change in specification "C". In this case the sensitivity between specification "A" and "C" would be of second order. In any event, the effect on specification "C" would be discussed as a first order sensitivity to a change in specification "B".

Table 3: Specification Sensitivity Summary

SPECIFICATION CHANGED	SPECIFICATION IMPACTED BY CHANGE											
	Centre Frequency	Bandwidth	Frequency Resolution	Frequency Accuracy	Frequency/ Phase Settling	Spurious	Phase Noise	Reference Stability	Reference Phase Noise	Size	Mass	Power Consumption
Centre Frequency	NA	0	0	1	0	0	2	0	0	1	0	1
Bandwidth	0	NA	1	0	0	3	0	0	0	1	1	1
Frequency Resolution	0	0	NA	0	0	0	0	0	0	0	0	0
Frequency Accuracy	0	0	0	NA	0	0	0	2	0	0	0	0
Frequency/Phase Settling	0	0	0	0	NA	0	0	0	0	0	0	0
Spurious	0	3	0	0	0	NA	0	0	0	0	0	0
Phase Noise	3	0	0	0	0	0	NA	0	3	0	0	0
Reference Stability	0	0	0	3	0	0	0	NA	0	0	0	0
Reference Phase Noise	0	0	0	0	0	0	3	0	NA	0	0	0
Size	0	0	0	0	0	0	0	0	0	NA	0	0
Mass	0	0	0	0	0	0	0	0	0	0	NA	0
Power Consumption	0	0	0	0	0	0	0	0	0	0	0	NA

NOTES:

"0" - Not sensitive. No change in synthesizer performance. No specification change is required.

"1" - Minor Sensitivity. The synthesizer performance would exhibit an insignificant change with respect to the degree to which the original performance was in/out of specifiation.

"2" - Intermediate sensitivity. The synthesizer performance would exhibit a change with respect to the degree to which the original performance was in/out of specification. However, the change would be insufficient to cause a previously compliant condition to beome non-compliant and vice-a-vera.

"3" - Major sensitivity. The synthesizer performance would exhibit a very significant change with respect to the degree to which the original performance was in/out of specification. The change would be sufficient to cause a previously compliant condition to become non-compliant and vice-a-versa.

NA - Not Applicable

The sensitivity of the specifications to each other depends heavily on the way in which the synthesizer is implemented. For this reason the sensitivity analysis is only valid for the selected synthesizer approach. Other synthesizer approaches may yield radically different specification sensitivities.

A detailed discussion of the sensitivity of each specification follows.

6.3.1 Centre Frequency

A change in *centre frequency* of ±25% represents a reasonable range which covers most of the intended applications for the synthesizer. This degree of change was used to determine the sensitivity of the other specifications to a change in the *centre frequency*.

The synthesizers *bandwidth, frequency resolution, frequency and phase settling, spurious* levels, *reference phase noise*, *reference stability*, and *mass*, are not sensitive to a 25% change in the output frequency.

Frequency accuracy exhibits a minor sensitivity to a change in the output frequency. In fact, *frequency accuracy* is directly proportional to the *centre frequency*. A ±25% change in the *centre frequency* will result in approximately the same percentage change in *frequency accuracy*. The originally predicted *frequency accuracy* of the synthesizer was 3869 Hz, assuming a 5 year mission life, and exceeds the required 100 Hz accuracy. A 25% decrease in the *frequency accuracy* is not sufficient to meet the specification. Calibration of the synthesizer or the incorporation of a Rubidium frequency reference would still be required. In fact, calibration would be required at least once every 63 days rather than every 43 days. A 25% increase in the frequency accuracy would not rule out the possibility of calibration nor the use of an atomic standard. At the higher frequency of operation, the synthesizer would need to be calibrated more frequently (once every 37 days rather than every 43 days).

Phase noise exhibits an intermediate sensitivity to a 25% change in the output *centre frequency*. *Phase noise* is directly proportional to frequency. This means that the *phase noise* will decrease as the *centre frequency* is decreased. A ±25% change in the *centre frequency* will result in approximately ±3 dB change in the output *phase noise*. This represents a significant change, because the predicted phase noise at the original centre frequency was within the specification by a margin of only 3 dB, at the offset frequencies of 1 kHz and 1 MHz.

Size will exhibit a relatively minor sensitivity to the 25% change in the *centre frequency*. This is true because a relatively large margin exists between the estimated *size* (625 cc) and the specification (1000 cc). *Centre frequency* and *size* are inversely proportional to each other. As the *centre frequency* is increased the *size* usually decreases. A ±25% change in frequency would result in approximately a ±10% change in *size*.

DC *power consumption* is directly proportional to the *centre frequency*. This results because the efficiency of the microwave amplifiers decreases with increased operating frequency. The DC *power consumption* of the other components will not change with operating frequency. The resulting change in the DC *power consumption* of the amplifiers, caused by a ±25% change in the *centre frequency*, would result in approximately a ±5% change in the overall DC *power consumption*. This represents a minor sensitivity of *power consumption* to a change in the *centre frequency*, because the predicted power consumption of 12.75 watts is well within the requirement of 15 watts.

6.3.2 Bandwidth

A substantial change in the *bandwidth* specification would be ±50% of the original value. This represents a reasonable range that would cover most foreseeable applications.

Specifications which are not sensitive to a 50% change in the *bandwidth* specification include, *frequency accuracy, frequency and phase settling, reference stability, phase noise,* and *reference phase noise.*

A 50% change in *bandwidth* would require the same percentage modification to the bandwidth expansion factor in the upconverter. Currently, to achieve the specified 1 GHz *bandwidth* the upconverter provides a 4-times bandwidth expansion factor. Decreasing the *bandwidth* specification by 50% to a value of 500 MHz would require a bandwidth expansion factor of only 2-times. This would be accomplished by removing one of the frequency doubler stages. Similarly, increasing the *bandwidth* specification by 50 % to 1.5 GHz would require increasing the bandwidth expansion factor from 4-times to 6-times. This could be accomplished by replacing one of the frequency doublers with a frequency tripler.

Modification of the upconverters bandwidth expansion factor will directly impact the frequency resolution of the synthesizer. Specifically, a 50% change in the bandwidth expansion factor will result in a 50% change in the *frequency resolution*.

The resulting change in the *frequency accuracy* would be 0.46 Hz which is insignificant when compared to the current margin between the predicted performance and the requirement. The required resolution is 200 Hz and the predicted performance is 0.92 Hz. Obviously, the *frequency resolution* specification exhibits a very minor sensitivity to a 50% change in the *bandwidth* specification.

Spurious levels are directly proportional to a change in the *bandwidth* specification. Decreasing the bandwidth expansion factor from four-times to two-times would result in a 6 dB decrease in the output spurious levels. Similarly, increasing the bandwidth expansion factor from four-times to 6-times would result in a 3.5 dB increase in the output spurious levels. Since the predicted *spurious* performance exceeds the current specification by 5 dB, the *spurious* level specification exhibits a major sensitivity to a 50% change in the bandwidth specification.

The necessary removal and or replacement of the frequency multipliers, to accommodate the bandwidth specification change, will result in little or no change in the *size, mass* and DC *power consumption* of the synthesizer. Removing one of the frequency multipliers will change the frequency plan and require at least one new local oscillator frequency. This new local oscillator can either be realized by a new frequency multiplication scheme or an additional phase locked oscillator. The reduction in *mass, size* and DC *power consumption* gained by removing the multiplier and its associated preamp, will be offset by the increased local oscillator complexity, and will result in little or no net change to these parameters. Replacing one of the frequency doublers with a tripler will also change the frequency plan. However, this can be accomplished with existing hardware or by direct replacement of some parts with similar components. Since the replacement parts will be of comparable size and mass and similar DC power consumption no net effect on these parameters will occur. The predicted *size, mass*, and *power consumption* are well within their respective specifications. Since a *bandwidth* specification change of 50% can be accommodated with little impact to the *size, mass*, and *power consumption*, then by definition , these specifications exhibit only a minor sensitivity to the *bandwidth* specification.

6.3.3 Frequency Resolution

The predicted *frequency resolution of* the synthesizer is 0.92 Hz, which meets the required 200 Hz resolution with significant margin. An order of magnitude change in the *frequency resolution* specification can be tolerated by the current design with no required modifications. All of the synthesizer specifications are not sensitive to an order of magnitude change in the *frequency resolution* specification.

6.3.4 Frequency Accuracy

The estimated *frequency accuracy* of the synthesizer (3869 Hz over five years) exceeds the 100 Hz specification by a significant amount. While many frequency hopping communications systems would operate quite satisfactorily with a 1 kHz frequency accuracy, there is little to be gained by requiring less than 100 Hz accuracy. For this reason, the sensitivity was determined for a degraded rather than an improved *frequency accuracy*.

The required *reference stability* for the synthesizer to maintain a *frequency accuracy* of 100 Hz over a 5 year period is on the order of 1e-12/day. This exceeds the specified reference stability of 1e-10/day by two orders of magnitude! A change of one order of magnitude in the *frequency accuracy* from 100 Hz to 1 kHz would require a *reference stability* of 1e-11/day. This is one order of magnitude smaller than the specified reference stability, which represents a significant change, with respect to, the two orders of magnitude that the required stability exceeds the specified stability. From our definition of sensitivity, this constitutes a intermediate sensitivity of the *reference stability* specification to the *frequency accuracy* specification.

All other specifications are not sensitive to a change in the *frequency accuracy* specification. However, the *centre frequency* does exhibit a second order sensitivity to the *frequency accuracy* (i.e . the maximum *centre freqency* to maintain the required *frequency accuracy* depends on the r*eference stability*).

6.3.5 Settling Characteristics

The synthesizer output will settle to the within the required frequency, phase, and amplitude levels in less than 100 nanoseconds. This meets the required settling time of 900 nanoseconds with significant margin. An order of magnitude change, in any or all of the required *settling characteristics*, can be tolerated by the current design with no required modifications. All of the synthesizer specifications are not sensitive to an order of magnitude change in the *settling characteristics* specification.

6.3.6 Spurious Levels

Since the selected synthesizer implementation cannot achieve the required *spurious* output level, a ±1 dB change in the *spurious* specification is considered to be substantial.

All specifications, with the exception of *bandwidth*, are not sensitive to a change in the spurious level specification.

The *spurious* performance of the synthesizer is intimately related to the bandwidth expansion factor used in the upconverter. Two frequency doublers provide a 4-times bandwidth expansion factor to yield a *bandwidth* of 1 GHz, which meets the specified requirement. However, this is accomplished at the expense of *spurious* performance. The predicted maximum *spurious* output of the synthesizer is -30 dBc rather than the required -35 dBc. Changing the *spurious* specification by ±1 dB would require that the bandwidth expansion factor, and hence the *bandwidth*, be reduced in half. This would result in a signal *bandwidth* of 500 MHz which is half of the required *bandwidth*. By definition, this demonstrates that the *bandwidth* specification exhibits a major sensitivity to the *spurious* level specification.

6.3.7 Phase Noise

The *phase noise* specifications given in Table 1 are reasonable requirements for most communications systems. In practice most applications can tolerate a ±10 dB deviation from these levels. This degree of change constitutes a substantial change in the *phase noise* specification, sufficient enough to use in the sensitivity analysis.

A 10 dB decrease in the *phase noise* specification would require that the operating *centre frequency* be reduced to at least half of it current value. On the other hand, a 10 dB increase in the *phase noise* specification would not require any change in the operating *centre frequency*. Overall, the *centre frequency* specification exhibits a major sensitivity to a 10 dB change in the *phase noise* specification.

For every ±1 dB change in the *reference phase noise*, at offset frequencies less than 100 KHz, a ±1 dB change in the output *phase noise* occurs. At higher frequencies the output *phase noise* is proportional to the noise of the VCO used in the PLL, rather than the *reference phase noise*. The required output *phase noise* at the 1 KHz offset frequency is -66 dBc. To meet this requirement, the worst case *reference phase noise* cannot exceed -127 dBc at the same offset frequency. This exceeds the required *reference phase noise* specification of -130 dBc by 3 dB, at a 1 KHz offset frequency. A 10 dB improvement in the output *phase noise* requirement will require at least a 10 dB improvement in the *reference phase noise* to maintain compliance with the new specification. This translates to a required maximum *reference phase noise* of -137 dBc. Similarly, a degradation of 10 dB in the output *phase noise* specification will require a maximum *reference phase noise* of -117 dBc.

A change of ±10 dB in the required *reference phase noise*, which originally demonstrated only a 3 dB margin to the specification, constitutes a major sensitivity to the output *phase noise* specification.

All remaining specifications are not sensitive to any change in the output *phase noise* specification.

6.3.8 Reference Stability

The specified *reference stability* of 1E-10 aging/day is easily achieved by an Oven-Controlled Crystal Oscillator (OCXO). A slightly cheaper reference would be a Temperature-Compensated Crystal Oscillator (TCXO) which typically exhibit 1E-9 aging/day. If stabilities better than 1E-10 aging/day are desired, a Rubidium standard must be used. Rubidium based oscillators possess a stability of 1e-12 aging/day. A range of 1E-9 aging/day to 1E-12 aging/day represents a reasonable restriction on the reference stability specification.

This range was used to determine the sensitivity of the various synthesizer parameters to the *reference stability* specification.

The *frequency accuracy* is the only parameter which is sensitive to a change in the *reference stability* specification. The estimated *frequency accuracy* of the synthesizer (3869 Hz over five years) exceeds the 100 Hz specification by a significant amount. Degrading the *reference stability* to 1E-9 aging/day would yield a *frequency accuracy* of 38.69 KHz. This represents an order of magnitude degradation in the *frequency accuracy*. A *reference stability* of 1E-12 aging/day would result in a *frequency accuracy* of 0.0212 Hz/day, or 38.69 Hz over a five year period. This would meet the required *frequency accuracy* specification of 100 Hz. From our definition of sensitivity, this constitutes a major sensitivity of the *frequency accuracy* to the *reference stability* specification.

6.3.9 Reference Phase Noise

The *reference phase noise* specification given in Table 1 is very close to the best that is practically achievable. Improving the *reference phase noise* specification is not practical. However, a 10 dB degradation in the reference phase noise is practical. To determine the sensitivity of the various parameters of the synthesizer to the *reference phase noise*, a degradation of 10 dB at all offset frequencies of the reference was used.

Only the synthesizers output *phase noise* is sensitive to a change in the *reference phase noise* specification. A degradation of 10 dB in the *reference phase noise* will result in a 10 dB degradation in the synthesizers *phase noise*, but only at offset frequencies less than about 100 KHz. At the higher offset frequencies the synthesizers *phase noise* is limited by the VCO phase noise of the PLL. At a 1 KHz offset frequency the synthesizer *phase noise* will be approximately -69 dBc, which is only 3 dB better than the requirement of -66 dBc. A 10 dB degradation in the *phase noise* will exceed the specification by 7 dB at the 1 KHz offset frequency. This stipulates that the output *phase noise* demonstrates a major sensitivity to the *reference phase noise*, at offset frequencies less than 100 KHz. At higher offset frequencies, changes in the *reference phase noise* will have no effect on the synthesizer *phase noise*.

6.3.10 Size

The predicted *size* of the synthesizer is 625 cc which meets the required *size* of 1000 cc with significant margin. A factor of two-thirds reduction in the *size* specification can be tolerated by the current design with no required modifications. All of the synthesizer specifications are not sensitive to a factor of two-thirds change in the *size* specification.

6.3.11 Mass

The predicted *mass* of the synthesizer is 1.4 kg which meets the required *mass* of 1.8 Kg with significant margin. A 20% reduction in the *mass* specification can be tolerated by the current design with no required modifications. All of the synthesizer specifications are not sensitive to a 20% change in the *mass* specification.

6.3.12 Power Consumption

The predicted *power consumption of* the synthesizer is 12.75 watts which meets the requirement of 15 watts with significant margin. A 15% reduction in the *power consumption* specification can be tolerated by the current design with no required modifications. All of the synthesizer specifications are not sensitive to a 15% change in the *power consumption* specification.

7.0 CANADIAN CONTENT

Many of the components required to build the synthesizer are not available in CANADA. This necessitates that the majority of the parts must be procured from the US. No foreign export restrictions are presently in effect on any of the required components.

However, CANADA does have significant expertise in the manufacture of MICs. COM DEV, as well as SPAR and MPR, have demonstrated significant capability in the manufacturing of MICs. These resources will be utilized to the fullest extent possible.

8.0 CONCLUSIONS

The purpose of this study was to conduct a comprehensive investigation into potential EHF SATCOM payload frequency-hopping synthesizer solutions. The primary objective was to conduct a specification sensitivity analysis for the development of a payload frequency-hopping synthesizer. In particular, the viability of implementing a synthesizer with the target specifications given in Table 1 was investigated. An impact and sensitivity assessment of changes to each of the individual specifications on all other requirements was performed.

A literature review of relevant articles on the analysis and design of frequency-hopping synthesizers was conducted. From information extracted in this review three frequency synthesizer implementations which could potentially meet the requirements of Table 1 were devised. A comparison of these three synthesizers revealed that the best solution was to use the implementation given in Figure 1. This synthesizer consists of a hybrid of Direct Digital Synthesis (DDS) and Direct Analogue Synthesis (DAS) techniques.

A detailed analysis of the preferred synthesizer approach revealed that it is viable to design and build a payload frequency-hopping synthesizer which will meet all of the given requirements. However, the synthesizer will not currently meet the required *spurious* and *frequency accuracy*. The result will be a degradation in the system dynamic range and noise figure, which will necessitate a reduction in user traffic and data rates. Performance improvements in the *spurious* levels and the *frequency accuracy* are feasible.

The *spurious* performance is limited by the dynamic linearity of the DAC used in the DDS. Advancements in DAC technology are currently in process and can potentially decrease the *spurious* to the required levels. The probability that a new DAC product will be available within the next two years is very high.

No synthesizer implementation can achieve the required *frequency accuracy* with the given *reference stability*. Calibration, or an improved *reference stability* is required to maintain the *frequency accuracy* over the synthesizer lifetime.

The results of the specification sensitivity analysis indicated that only a few of the specifications are highly sensitive to each other. These include the following:

1. *Centre Frequency* is sensitive to the *phase noise* specification.
2. *Bandwidth* is sensitive to the *spurious* specification.
3. *Frequency accuracy* is sensitive to the *reference stability*.
4. *Spurious* levels are sensitive to the *bandwidth* requirements.
5. *Phase noise* is sensitive to the *reference phase noise* at offset frequencies less than 100 KHz.
6. *Reference phase noise* is sensitive to the output *phase noise* requirements at offset frequencies less than 100 kHz.

The sensitivity analysis is valid only with regard to the selected synthesizer approach. Other synthesizers may or may not exhibit the same sensitivity characteristics.

9.0 RECOMMENDATIONS

COM DEV recommends the design, build, and test of a breadboard synthesizer using the approach identified in this study. The implementation described in this report represents an advancement over currently available space qualified frequency-hopping EHF sources. Demonstrating the capability to build the synthesizer for space-based applications will help delineate Canada as a leader in EHF SATCOM spacecraft technology. In addition, the breadboard build would serve the following critical purposes:

1. The verification of electrical performance and mechanical characteristics.
2. Reduction of the risk involved with the use of advanced DDS technology.
3. The identification and development of critical assembly processes.

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APPENDIX A

Task 1 Report

COM DEV

155 Sheldon Drive, Cambridge, Ontario Canada N1R 7H6

FASSET

REVISION RECORD

LTR	ECN NO	DATE	APP SIGN	CADM RELEASE

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Function: Proj Manager
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TASK 1 OF THE EHF SATCOM PAYLOAD FREQUENCY SYNTHESIZER STUDY

CADM RELEASE CM 10

PROJ. NO. 5085

DOCUMENT NO.	REV.	CAGE CODE 38101	A
TNO/SKN/5085/001	-	SHEET 1 OF 9	

SHEET ISSUE RECORD

Rev. - of the document comprises the following pages at the revisions shown.

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	DOCUMENT NO.	REV.	CAGE CODE
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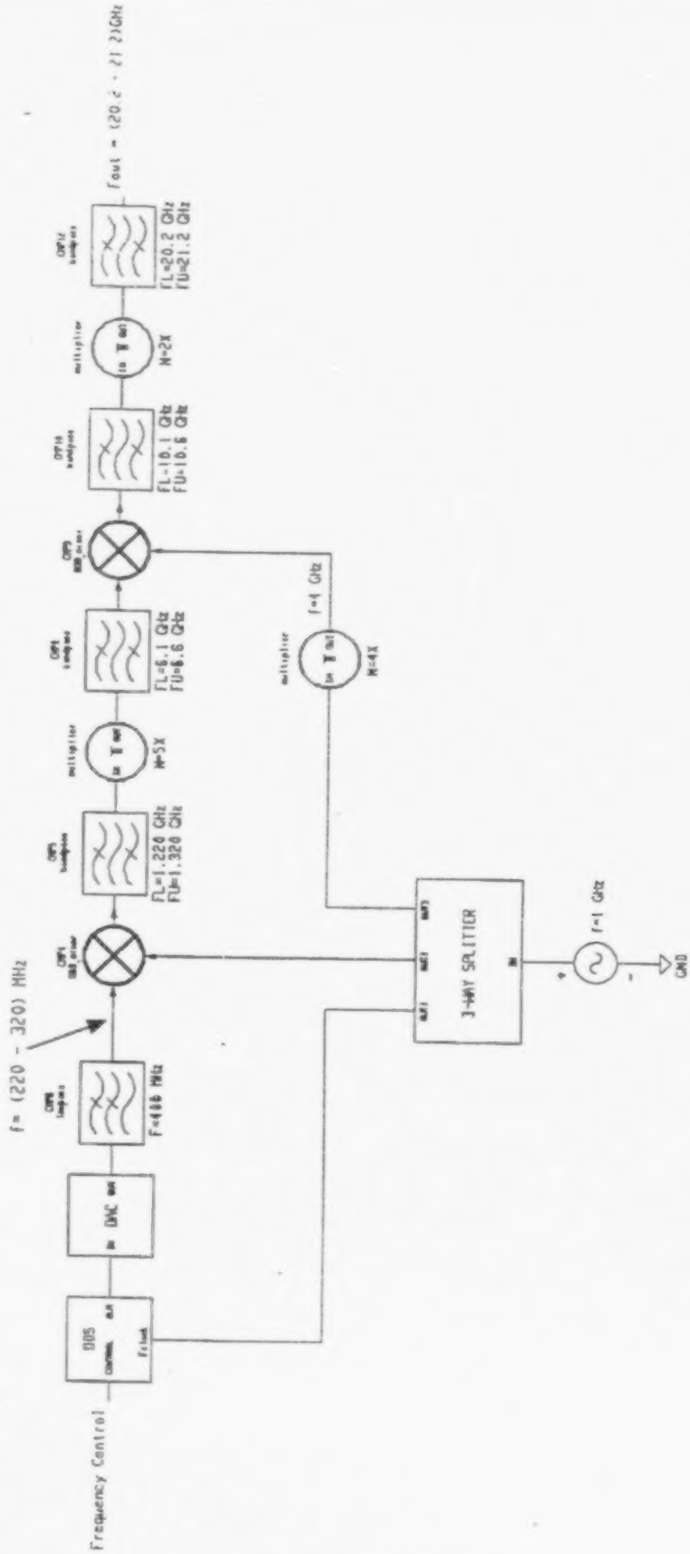
COMDEV has conducted a literature review of relevant articles on the analysis and design of frequency-hopping synthesizers. The review involved more than 30 papers (see list attached) which discussed, Direct Digital Synthesis (DDS), Direct Analog Synthesis (DAS), Phase-Locked Loop (PLL), and hybrid approaches to frequency synthesis. Some of the papers gave actual solutions to the fast-hopping synthesizer problem while others discussed the topic of frequency synthesis on a more general level. From this effort COMDEV has arrived at four potential payload frequency-hopping synthesizer solutions. Block diagrams of each of these four synthesizer options are given on the attached pages.

OPTION 1 is a DDS and DAS hybrid synthesizer. A state-of-the-art GaAs DDS which runs at a clock frequency of 1 GHz provides an output signal between 220 MHz and 320 MHz in less than 1 Hz steps. The 1 GHz clock is also used to drive a mixer which up-converts the DDS signal to 1270 MHZ +/- 50 MHz. This signal is than multiplied by 5 to provide bandwidth expansion to 500 MHz, and centre frequency translation to 6.35 GHz. Multiplying the 1 GHz clock by four provides a 4 GHz local oscillator which allows up-conversion to a centre frequency of 10.35 GHz. A frequency doubler provides the required 20.2 GHz to 21.2 GHz output frequency range.

OPTION 2 utilizes a fast-locking PLL to provide coarse frequency tuning in 60 MHz steps. The fine frequency tuning is provided by a low frequency DDS. The DDS is driven by a 60 MHz clock which generates an output frequency of 19 MHz +/- 5 MHz. A two stage up-converter translates the DDS output to a centre frequency of 4.664 GHz, with a corresponding bandwidth of 60 MHz. The bandwidth expansion is created by the 6X frequency multiplier. The PLL utilizes a fast-acquisition circuit to lock to the 60 MHz reference. The output of the PLL is programable between 5.42 GHz and 5.90 GHz in 60 MHz steps. Mixing of the DDS up-converted signal with the PLL output gives more than 500 MHz frequency coverage at a centre frequency of 10.35 GHz. Frequency doubling generates the required 20.2 GHz to 21.2 GHz output frequency range.

OPTION 3 is simply a PLL which is locked to a DDS generated reference frequency. This allows fine tuning of the PLL output frequency. Coarse tuning is provided by adjusting the division ratio within the PLL. The required 20.2 GHz to 21.2 GHz output frequencies are generated by up-converting the PLL output.

OPTION 4 is a PLL and DDS hybrid type synthesizer. A low frequency DDS is used within the closed-loop of the PLL to offset the VCO output before comparison with the reference frequency. This allows fine tuning of the PLL output. Coarse tuning is provided by adjusting the PLL division ratio.


Frequency Control
DDS
CONTROL
OUT
Fclock
IN
DAC
OUT
F=400 MHz
f= (220 - 320) MHz
FL=1.220 GHz
FU=1.320 GHz
multiplier
N=5X
FL=6.1 GHz
FU=6.6 GHz
multiplier
N=4X
f=4 GHz
FL=10.1 GHz
FU=10.6 GHz
multiplier
N=2X
FL=20.2 GHz
FU=21.2 GHz
fout = (20.2 - 21.2)GHz
3-WAY SPLITTER
IN
OUT1
OUT2
OUT3
f=1 GHz
+
-
GND

Option 1: DDS/Direct Analogue Frequency Synthesizer

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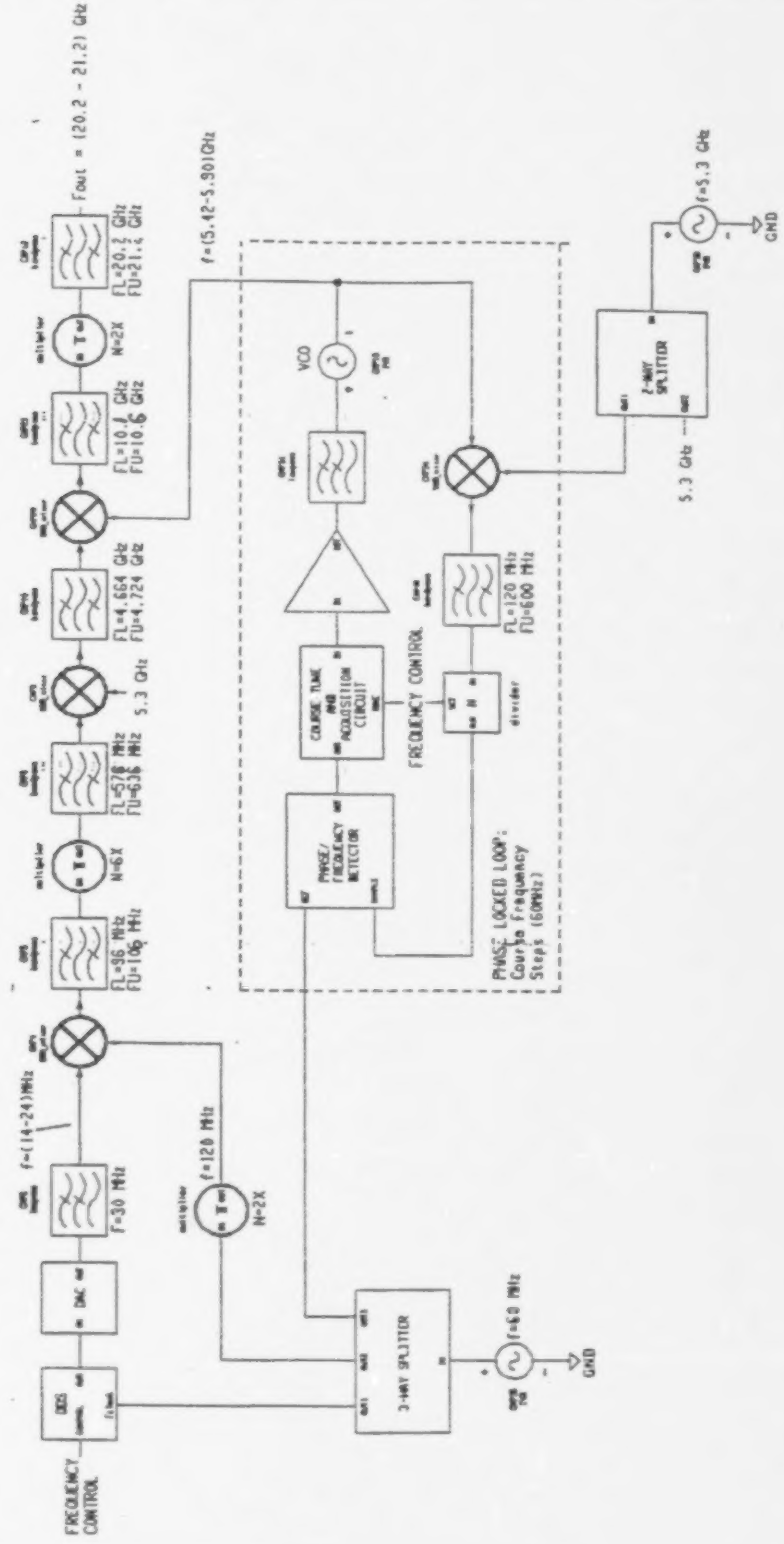
FREQUENCY CONTROL
DDS
DAC
F=30 MHz
f=(14-24) MHz
FL=96 MHz
FU=106 MHz
multiplier
N=6X
FL=576 MHz
FU=636 MHz
5.3 GHz
FL=4.664 GHz
FU=4.724 GHz
FL=10.1 GHz
FU=10.6 GHz
multiplier
N=2X
FL=20.2 GHz
FU=21.4 GHz
Fout = (20.2 - 21.2) GHz
f=(5.42-5.901)GHz
VCO
COURSE TUNE AND ACQUISITION CIRCUIT
PHASE/FREQUENCY DETECTOR
FREQUENCY CONTROL
divider
FL=120 MHz
FU=600 MHz
PHASE LOCKED LOOP:
Course Frequency
Steps (60MHz)
2-WAY SPLITTER
5.3 GHz
f=5.3 GHz
GND
multiplier
f=120 MHz
N=2X
3-WAY SPLITTER
f=60 MHz
GND

Option 2: DDS/PLL Up-Converting Frequency Synthesizer

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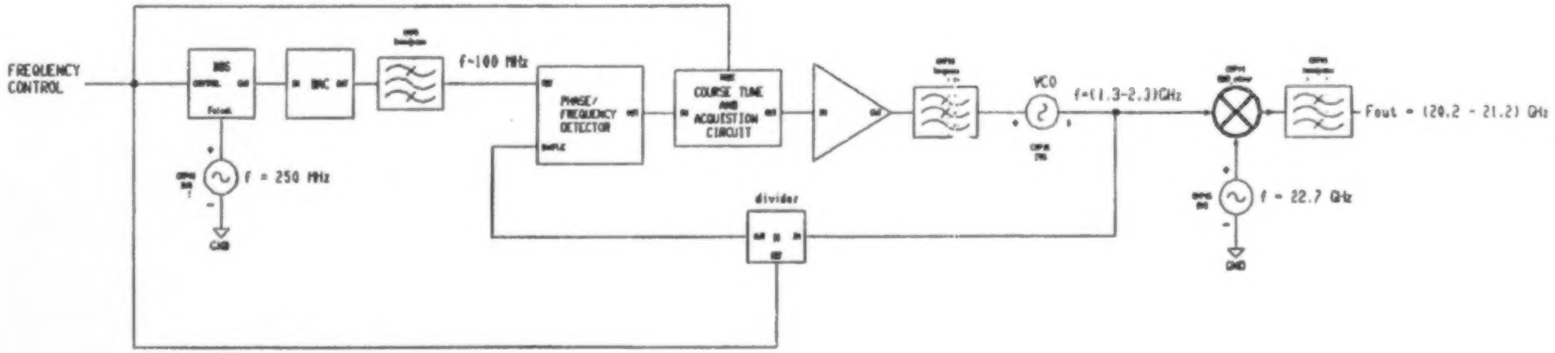
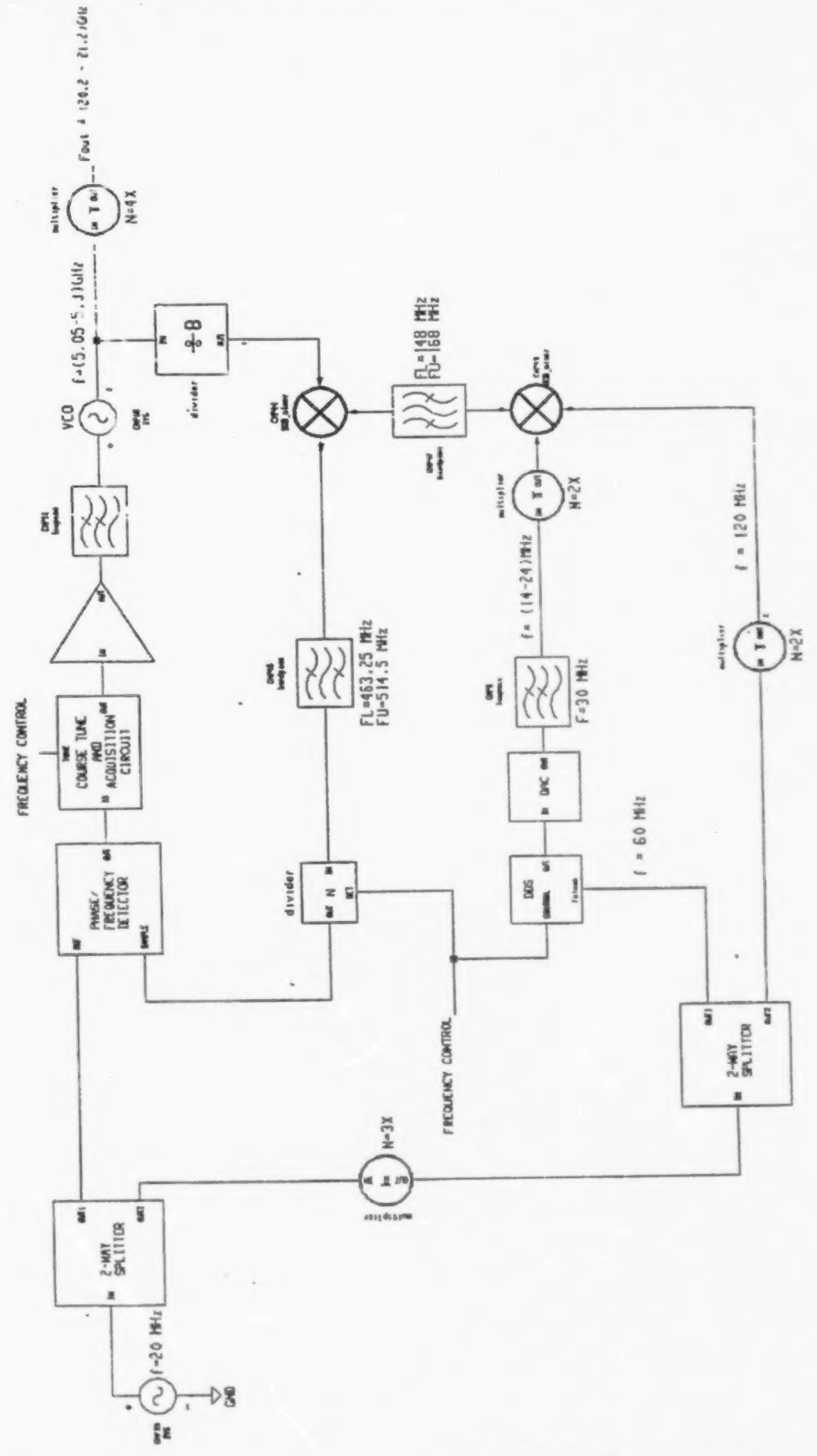

FREQUENCY CONTROL
DDS
f = 250 MHz
GND
DAC
f~100 MHz
PHASE/ FREQUENCY DETECTOR
COURSE TUNE AND ACQUISTION CIRCUIT
VCO
f=(1.3-2.3)GHz
divider
f - 22.7 GHz
GND
Fout = (20.2 - 21.2) GHz

Option 3: DDS Driven PLL Frequency Synthesize


Fout = (20.2 - 21.2)GHz
multiplier
N=4X
f=(5.05-5.3)GHz
VCO
divider
÷8
FL=148 MHz
FU=168 MHz
FREQUENCY CONTROL
COURSE TUNE AND ACQUISITION CIRCUIT
PHASE/ FREQUENCY DETECTOR
FL=463.25 MHz
FU=514.5 MHz
divider
N
f = (14-24)MHz
N=2X
F=30 MHz
DAC
DDS
f = 60 MHz
f = 120 MHz
N=2X
FREQUENCY CONTROL
2-WAY SPLITTER
N=3X
multiplier
2-WAY SPLITTER
f=20 MHz
GND

Option 4: PLL With DDS Frequency Offset

DOCUMENT NO.	REV.	COM DEV
TNO/SKN/5085/001	—	SHEET 7

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APPENDIX B

Task 2 Report

COM DEV

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REVISION RECORD

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TASK 2 of the EHF SATCOM Payload Frequency Synthesizer Study

CADM RELEASE CM 10		PROJ. NO. 5085
DOCUMENT NO.	REV.	CAGE CODE 38101
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1.0 INTRODUCTION

The Task 1 report of the EHF SATCOM Payload Frequency Synthesizer study suggested three potential implementations for the EHF SATCOM payload fast-hopping frequency synthesizer. Block diagrams of the proposed synthesizers are given in Figures 1, 2, and 3. Initial analysis of these options indicated that they could not meet the required spurious performance. Slight modifications were made to each of the options to improve their performance. The modified synthesizer implementations are given in Figures 4, 5, and 6. This report compares the three modified synthesizer options and selects one of the options for further detailed analysis and study.

2.0 COMPARISON

As stipulated by the SOW the three synthesizer architectures are compared on the basis of the following parameters:

1) signal bandwidth
2) frequency resolution
3) frequency accuracy
4) settling characteristics for phase and frequency
5) spurious performance
6) phase noise
7) required reference stability and phase noise
8) size
9) weight
10) power consumption
11) cost

Table 1.0 lists each of the above parameters with its associated specification. The estimated performance of the three synthesizer implementations are also listed in the table.

The required ***signal bandwidth*** of 1 GHz, at a centre frequency of 20.7 GHz, can be achieved by all three of the proposed synthesizers. Achieving the required signal outputs is accomplished at the expense of increased design complexity. In particular, Option 1 requires a high speed DDS, while the other two options require Phase Locked Loops (PLL) with a wide tuning bandwidth. The high speed DDS degrades spurious performance, and increases the DC power consumption. Qualification of the DDS to the required quality level poses additional technical risk. A fast settling PLL, with a wide tuning range, will require complex acquisition circuitry, and a VCO with an extremely low post-tuning drift.

The specified ***frequency resolution*** of 200 Hz, maximum, is easily achieved by all three of the synthesizer options. All options utilize a DDS to generate the required frequency steps. The resulting maximum frequency resolution will be, 1.8 Hz, 0.2 Hz, and 0.1 Hz, for options 1, 2, and 3 respectively.

The 100 Hz ***frequency accuracy*** is achieved by each of the three options, but at the expense of improved reference stability. Irrespective of the design approach used, the output frequency must always be locked to the reference frequency. The locking process causes a small change in the reference frequency to become a proportionately larger change in the output frequency. The resulting frequency deviation at the synthesizer output, will be the change in the reference frequency, multiplied, by the ratio of the output frequency to the reference frequency. The worst case frequency deviation will occur at the maximum output frequency of 21.2 GHz. The specified stability of the 5 MHz reference is 1E-10 aging/day. This would yield a worst case frequency drift of 2.12 Hz per day at the synthesizer output. Assuming a mission life of 5 years, the resulting worst case frequency accuracy would be 3869 Hz. To remain within 100 Hz, worst case, the frequency reference would require a stability of $<3\times10^{-12}$ aging/day, or for correction to be performed at least once every 45 days.

The ***settling time*** performance of Option 1 surpasses the remaining two options by an order of magnitude. The excellent switching time of option 1 is accomplished by the high speed DDS. The DDS will settle to the required frequency, phase, and amplitude, within 25 nsec. Allowing an additional 75 nsec for the amplitude settling associated with the various filters and amplifiers, a settling time of 100 nsec is feasible with the option 1 approach. Achieving the required 900 nsec settling time with option 2 and 3 will be extremely difficult. Both of these options incorporate a PLL which must be tunable over a large bandwidth. Complex acquisition circuitry is required to achieve fast frequency switching of a PLL that must maintain a large tuning range. In addition, a VCO that exhibits very low post tuning drift is required. Fast locking PLLs usually require large loop bandwidths and high open loop gains. This invariably leads to severe stability problems. Nonetheless, PLLs with less than 700 nsec settling times have been demonstrated.

The ***spurious performance*** of all three options should be dominated by the DDS generated spurious signals. The predicted levels of DDS generated spurious, at the synthesizer output, will be less than -30 dBc, -39 dBc, and -47 dBc, for Options 1, 2, and 3 respectively. This assumes that all other sources of spurious signals can be adequately suppressed. Spurious signals which originate from mixer intermodulation, and conducted and irradiated signal injection, can be kept below -60 dBc. This can be accomplished with appropriate filtering, signal level management, and enclosure design. The reference sidebands associated with PLLs is a spurious problem shared by both Options 2 and 3. The reference sidebands result from leakage of the reference signal through the loop filter and subsequent modulation of the VCO. Fast switching PLLs typically exhibit poor reference sideband levels, because of the required wide loop bandwidths. Increasing the loop filter order may reduce the reference sidebands, but at the expense of loop stability. Reduction of the reference sideband levels can be accomplished without additional loop filtering, but only with additional circuit complexity. It is assumed that sufficient sideband suppression can be provided to reduce the levels below the DDS generated spurious.

Options 1 and 2 will meet the required ***phase noise*** with the specified ***reference phase noise*** levels. Option 3 will not meet the required phase noise at the 1 Mhz frequency offset. Improving the reference phase noise will not improve the phase noise performance of Option 3, which is limited by the thermal noise floor, rather than the reference phase noise.

The required 100 Hz frequency accuracy cannot be achieved by any implementation with the specified ***reference stability***. Assuming a 5 year mission life, the required stability of the 5 MHz reference, to maintain a frequency accuracy of 100 Hz, is approximately 1E-12 aging/day. This level of stability can only be provided by a Cesium or Rubidium standard. An alternative to these atomic standards is to calibrate the synthesizer at regular intervals. With the specified reference stability of 1E-10 aging/day, calibration would be required at least once every 45 days.

All three synthesizer options will meet the specified ***size, weight, and power consumption*** requirements. Option 1 will be the smallest and lightest of the three, with Option 2 a close second, while Option 3 will be the largest and heaviest. The power consumption of Options 2 and 3 is expected to be roughly the same, at 12.5 W and 12.25 W respectively. Option 1 will consume about 1 W less than either of the two other options.

Option 1 will ***cost*** the least to develop. The expected cost of Options 2 and 3 will be roughly a factor of 1.5 to 2 times, and 2 to 2.5 times, more costly than Option 1, respectively. Option 3 is expected to be the most costly approach, because of the complexity of the required PLL. Cost estimates were derived strictly from the expected level of non-recoverable engineering (NRE) that would be required to produce a **prototype** synthesizer.

The comparison between the potential synthesizer approaches would be incomplete without considering qualification issues. Although Option 1 will provide the best performance, the required high speed DDS is not currently available at a space qualified level. New DDS products are currently in development. Qualification of these new products is anticipated within the next two years. In contrast, both Option 2 and 3 can be realized with components that have a history of high reliability. However, Option 2 will require a phase locked 22.5 GHz DRO, which will be difficult to procure at the required quality level. Furthermore, the relative additional complexity of Options 2 and 3, as compared to Option 1, may yield a lower reliability.

3.0 RECOMMENDATION

Of the three contending synthesizer approaches, Option 1 exhibits the best overall electrical and mechanical characteristics. It will cost the least, and imposes the lowest technical risk. Although Option 2 meets all of the specifications, the risk and cost associated with the development of a fast tuning PLL, is high. The fast tuning PLL proposed in Option 3, requires loop circuitry that is slightly more complex than that of Option 2. This makes option 3 the most technically risky, and the most costly, of the three alternatives. Furthermore, Option 3 cannot meet the phase noise requirements. Both Options 2 and 3 will be bigger, heavier, and consume more power than Option 1.

The only shortfall of the Option 1 approach is that it does not meet the required spurious performance of -35 dBc. The limiting factor on the spurious performance is the dynamic linearity of the DAC used in the DDS. The estimated spurious performance of Option 1 (i.e. -30 dBc) is based on the use of TRIQUINT's TQ6122 8 Bit, 1 GHz, DAC. The TQ6122 is specified to provide a dynamic linearity of better than -42 dBc. This is the best available performance from all commercially available DACs. Improvement in the spurious performance is possible, as new DACs with better dynamic linearity are currently in development. A four company consortium consisting of SCITEQ, TRIQUINT, MOTOROLA, and SANDIA LABS, are jointly involved in the design of a 14 bit high speed DAC. TRIQUINT will eventually market this product as the TQ6140. Samples of this part are currently available from TRIQUINT. Initial measurements have shown that the TQ6140 provides a dynamic linearity of better than -55 dBc, when clocked at 1 GHz. The TQ6140 should be available, on a commercial basis, sometime in the first quarter of 1994. The TQ6140 would improve the spurious performance of Option 1 to an impressive level of -43 dBc. SCITEQ is also independently developing a fully monolithic DDS which incorporates an on chip 10 bit DAC. This device has demonstrated a -52 dBc spurious performance at an 800 MHz clock rate. This product will be available on a sample basis in the fall of 1993. Incorporation of the new SCITEQ DDS in Option 1, would result in a maximum output spurious level of -40 dBc. Initial indications from the suppliers, suggest that these parts can be provided to space quality levels by early 1995.

The potential improvement offered by the new DAC technologies definitely delineates Option 1 as the best fast-hopping frequency synthesizer approach. COM DEV recommends Option 1 for approval by the Design Authority for further study.

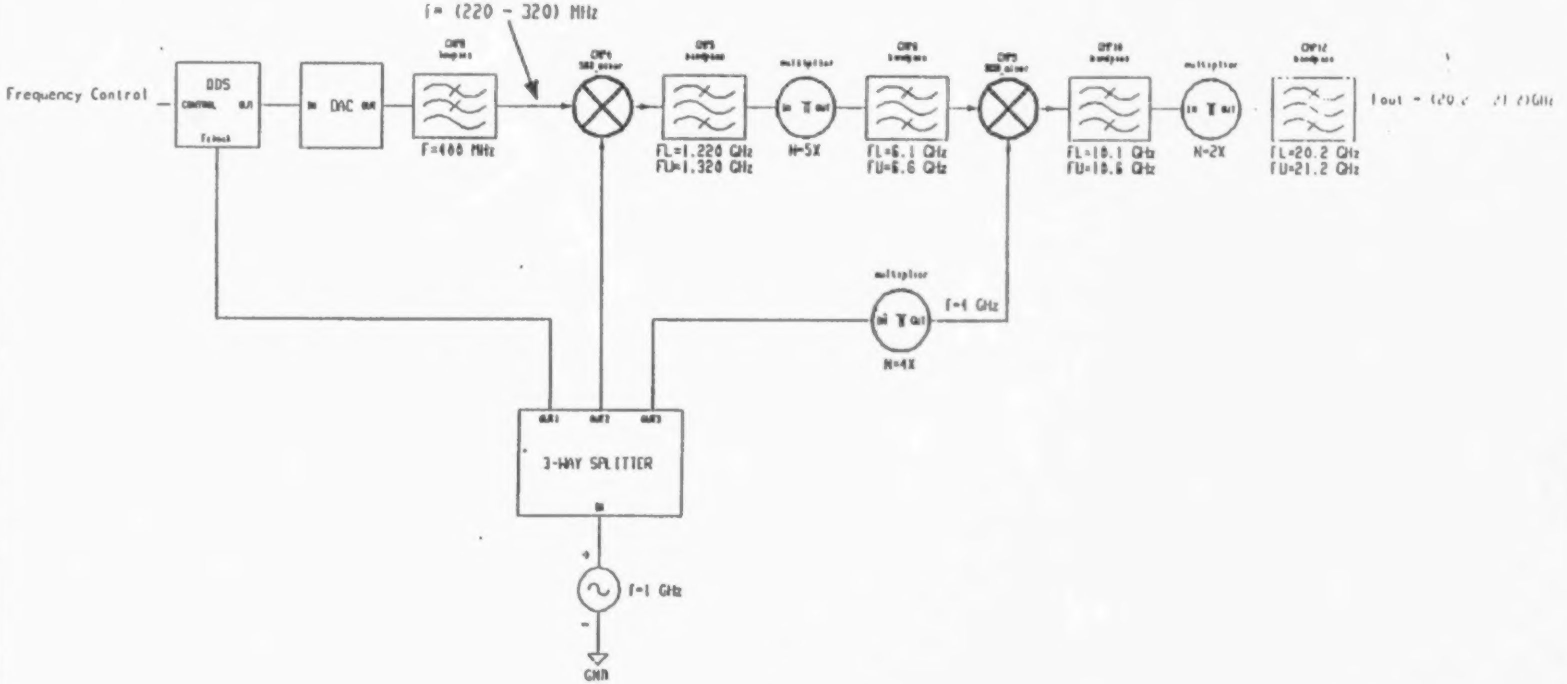
Frequency Control
DDS
CONTROL
OUT
DAC
bandpass
F=400 MHz
f= (220 - 320) MHz
FL=1.220 GHz
FU=1.320 GHz
multiplier
N=5X
FL=6.1 GHz
FU=6.6 GHz
CMP10
bandpass
FL=10.1 GHz
FU=10.6 GHz
multiplier
N=2X
CMP12
bandpass
FL=20.2 GHz
FU=21.2 GHz
Iout - (20.2 21.2)GHz
multiplier
f=4 GHz
N=4X
3-WAY SPLITTER
OUT1
OUT2
OUT3
IN
+
-
f=1 GHz
GND

Figure 1: Option 1 DDS/Direct Analogue Frequency Synthesizer

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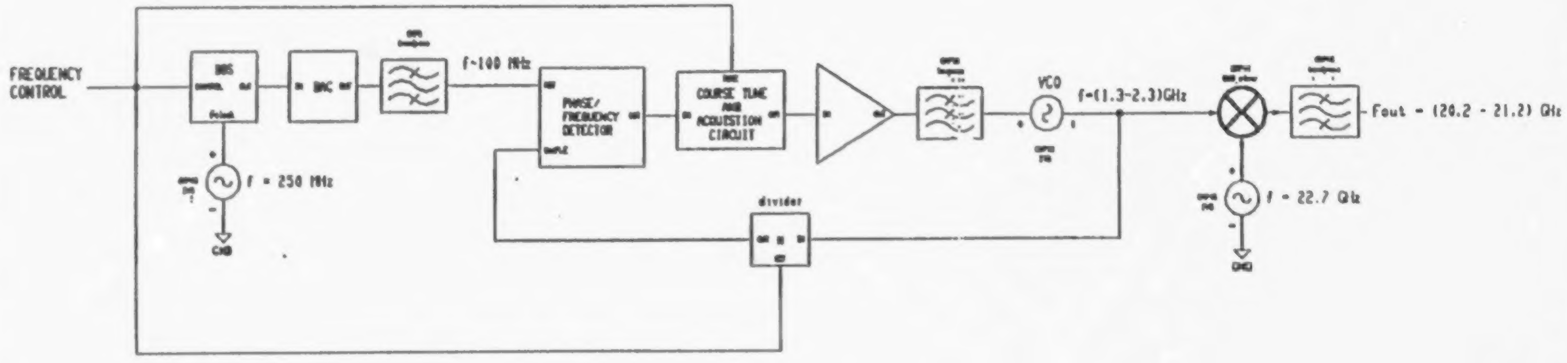
FREQUENCY CONTROL
DDS
f = 250 MHz
GND
DAC
f~100 MHz
PHASE/ FREQUENCY DETECTOR
COURSE TUNE AND ACQUISITION CIRCUIT
divider
VCO
f=(1.3-2.3)GHz
f = 22.7 GHz
GND
Fout = (20.2 - 21.2) GHz

Figure 2: Option 2 DDS Driven PLL Frequency Synthesizer

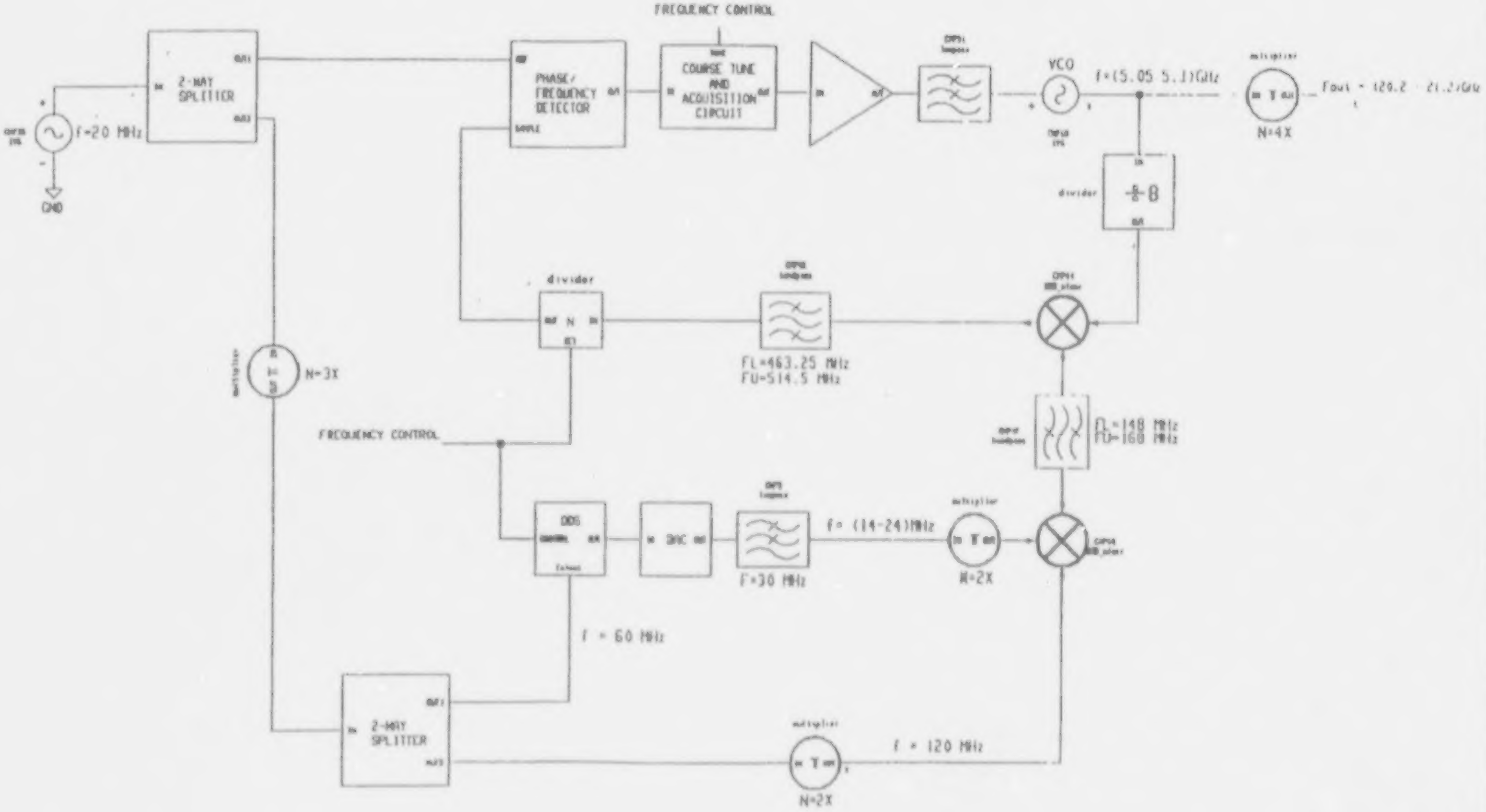
FREQUENCY CONTROL
2-WAY SPLITTER
f=20 MHz
GND
PHASE/ FREQUENCY DETECTOR
COURSE TUNE AND ACQUISITION CIRCUIT
VCO
f=(5.05 5.1)GHz
multiplier
N=4X
Fout = (20.2 - 21.2)GHz
divider
÷8
divider
N
FL=463.25 MHz
FU=514.5 MHz
FL=148 MHz
FU=168 MHz
N=3X
FREQUENCY CONTROL
DDS
DAC
F=30 MHz
f= (14-24)MHz
multiplier
N=2X
f = 60 MHz
2-WAY SPLITTER
multiplier
f = 120 MHz
N=2X

Figure 3: Option 3 PLL with DDS Frequency Offset

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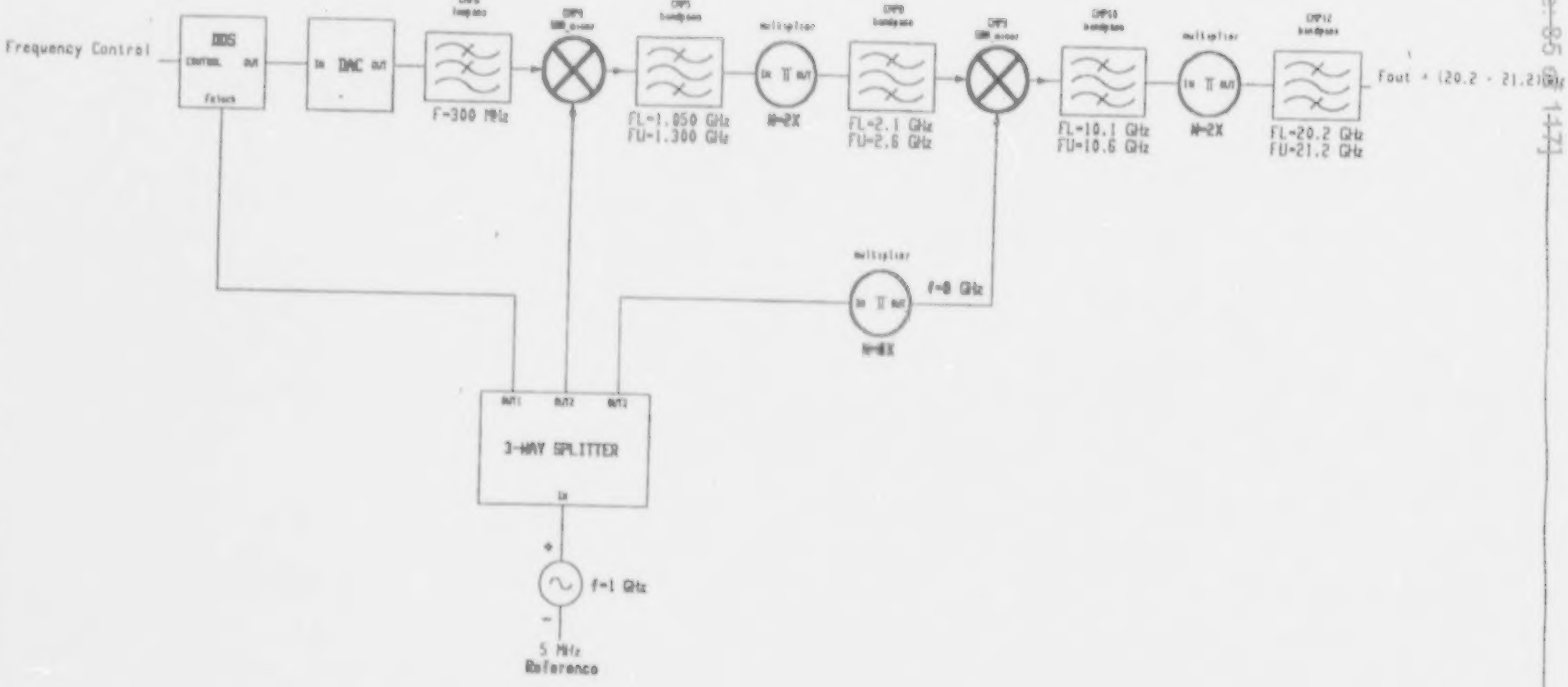
Frequency Control
DDS
CONTROL
OUT
Fclock
IN
DAC
OUT
lowpass
F=300 MHz
DBL_mixer
bandpass
FL=1.050 GHz
FU=1.300 GHz
multiplier
IN
OUT
N=2X
bandpass
FL=2.1 GHz
FU=2.6 GHz
DBL_mixer
bandpass
FL=10.1 GHz
FU=10.6 GHz
multiplier
N=2X
bandpass
FL=20.2 GHz
FU=21.2 GHz
Fout = (20.2 - 21.2)GHz
multiplier
f=8 GHz
N=8X
OUT1
OUT2
OUT3
3-WAY SPLITTER
IN
+
f=1 GHz
-
5 MHz
Reference

Figure 4: Option 1 (Modified) DDS/Direct Analogue Frequency Synthesizer

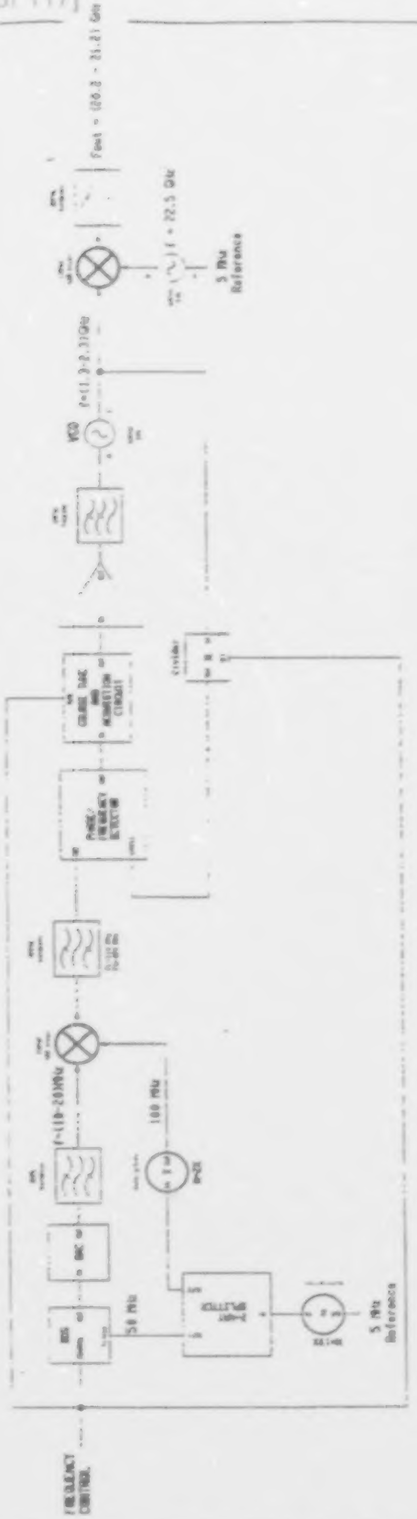
FREQUENCY CONTROL
DDS
DAC
50 MHz
f=(10-20)MHz
100 MHz
5 MHz Reference
2-WAY SPLITTER
PHASE/FREQUENCY DETECTOR
COARSE TUNE AND ACQUISITION CIRCUIT
DIVIDER
VCO
f=(1.3-2.3)GHz
f = 22.5 GHz
5 MHz Reference
Fout = (20.2 - 21.2) GHz

Figure 5: Option 2 (Modified) DDS Driven PLL Frequency Synthesizer

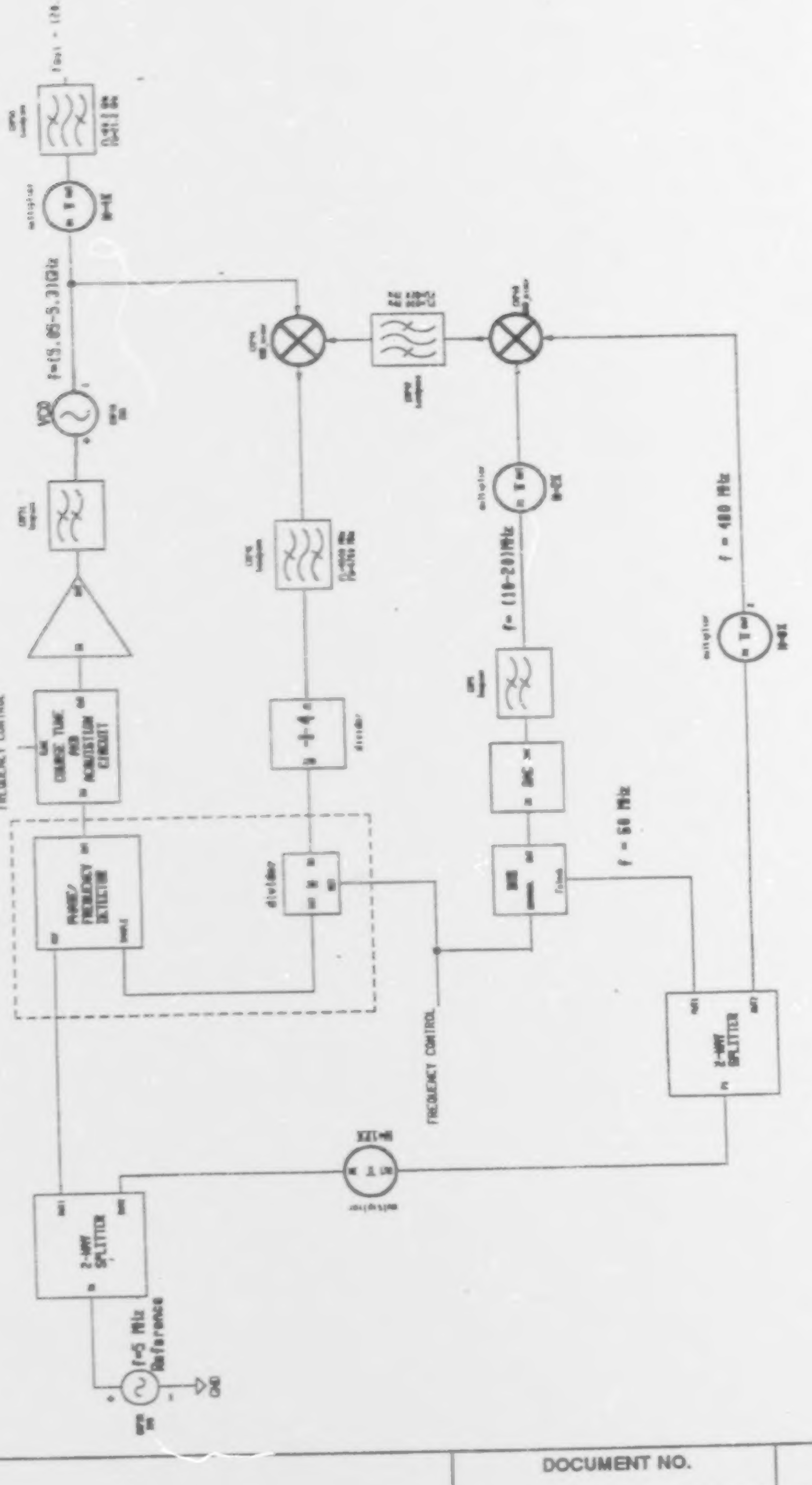
f=(5.05-5.31)GHz
VCO
multiplier
FREQUENCY CONTROL
COARSE TUNE AND ACQUISITION CIRCUIT
PHASE/ FREQUENCY DETECTOR
divider
÷4
DDS
DAC
f= (10-20)MHz
f = 60 MHz
f = 400 MHz
2-WAY SPLITTER
N=12X
f=5 MHz Reference
GND

Figure 6: Option 3 (Modified) PLL with DDS Frequency Offset

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Table 1: Table of Comparison between the Three Synthesizer Options

Serial	Parameter	Specification	Option 1	Option 2	Option 3
1	Signal Bandwidth	20.2 - 21.2 GHz	20.2 - 21.2 GHz	20.2 - 21.2 GHz	20.2 - 21.2 GHz
2	Frequency Resolution	<= 200 Hz	1.8 Hz	0.2 Hz	0.1 Hz
3	Frequency Accuracy	100 Hz	100 Hz	100 Hz	100 Hz
4	Settling Time <= 1KHz of target value <= 15 degrees of target value within 10% of target amplitude	<= 900 nSec	<= 100 nSec	<= 900 nSec	<= 900 nSec
5	Spurious Performance	<= -35 dBc	<= -30 dBc	<= -39 dBc	<= -47 dBc
6	Phase Noise	<= -66 dBc/Hz @ 1 kHz <= -108 dBc/Hz @ 1 MHz <= -118 dBc/Hz @ 1GHz	<= -66 dBc/Hz @ 1 kHz <= -108 dBc/Hz @ 1 MHz <= -118 dBc/Hz @ 1GHz	<= -66 dBc/Hz @ 1 kHz <= -108 dBc/Hz @ 1 MHz <= -118 dBc/Hz @ 1GHz	<= -66 dBc/Hz @ 1 kHz <= -90 dBc/Hz @ 1 MHz <= -118 dBc/Hz @ 1GHz
7	Reference Stability and Phase Noise (5 MHz Reference)	1E-10 aging/day -130 dBc/Hz @ 10 Hz -148 dBc/Hz @ 1 kHz	1E-12 aging/day -130 dBc/Hz @ 10 Hz -148 dBc/Hz @ 1 kHz	1E-12 aging/day -130 dBc/Hz @ 10 Hz -148 dBc/Hz @ 1 kHz	1E-12 aging/day -130 dBc/Hz @ 10 Hz -148 dBc/Hz @ 1 kHz
8	Size	1000 cc	545 cc	675 cc	785 cc
9	Weight	1.8 Kg	1.25 Kg	1.5 Kg	1.75 Kg
10	Power Consumption	15 W	11.5 W	12.5 W	12.25 W
11	Cost	-	1	1.5 - 2	2 - 2.5

APPENDIX C

Synopsis of Relevant Papers

The following synopses are extracted directly from either the abstract or summary of the cited papers.

[1] Alexovich, J.R., & R.M. Gagliardi, "Frequency Synthesizer Transient Effects in FH-FSK", MILCOM 86: IEEE Military Communications Conference. vol. 3, pp. 40.5/1-5, 1986.

"Agile frequency synthesizers have been proposed for accomplishing the frequency-hopping and dehopping in FH-FSK communications. Since the design of such synthesizers generally involve divide-down phase-lock loops, transients exist that limit the ability of the loop to hop rapidly over the hopping band. These transients lead to effective energy loss that degrades the resulting decoding performance. In this paper, hopping transients are studied in terms of their dynamical equations, their relation to key loop parameters, and their effect on decoding operations. The importance of pre-tuning is shown. Suggested techniques to combat the transient loss, as delaying the decoder integration start-time, or ping-ponging two synthesizers, are evaluated."

[2] Balanov, O.A., & A.I. Kabanov, "The Principles of the Construction of Microwave Frequency Synthesizers", Electrosvyaz, vol. 41, no. 4, pp. 53-56, April 1987.

"Each year, frequency synthesis technology finds ever increasing applications in different areas of radio engineering. The saturation of the decameter and meter bands by radio facilities of various kinds has led to the need to develop frequency synthesizers (FS) in the decimeter and centimeter wavebands, i.e., the microwave frequency band (1,2,6,8). The shift of the frequency band into the microwave band occurs at a time when there is a concurrent tightening of the requirements imposed on the operational-technical characteristics of the FS. In many cases, the use of methods for constructing meter-wave synthesizers in the microwave frequency band has failed to yield the required technical characteristics.

The purpose of this paper is to generalize and classify the various systems of microwave frequency synthesizers, to carry out a brief analysis of the principles of the construction of FS based on systems of phase-locked automatic frequency control (PAFC), and to correlate various synthesizer structures with respect to the fluctuation level in the output signal spectrum."

[3] Basawapatna, G.R., "Microwave Supercomponents Evolve into Higher Performance Synthesized Systems", MSN, vol. 19, no. 8, pp. 26-34, August, 1989.

"Three major classes of frequency synthesis are reviewed and performance comparisons made. Advances in synthesizer designs are being achieved by incorporating the best available signal processing components into compact packages."

[4] Benn, H.P., & W.J. Jones, "A Fast Hopping Frequency Synthesizer", Second International Conference on Frequency Control and Synthesis, no. 303, pp. 69-72, April 1989.

"This paper gives a description of a fast hopping frequency synthesizer whose main features make it ideal for use in agile radar and spread spectrum communications systems. These include very fast switching speed coupled with close channel spacing, low phase noise and high spectral purity. Using conventional phase locked loop methods a limitation of channel spacing is imposed if optimum phase noise and fast switching speed are required. This has been overcome by incorporating a direct digital synthesizer, driven from a high frequency fundamental surface acoustic wave resonator oscillator (SAWRO) exhibiting very low noise."

[5] Berglund, C.D., *et al.*, "High Speed Synthesizers for Satellite Application", AIAA 11th Communications Satellite Systems Conference, pp. 352-60, March, 1986.

"High-speed wide-band microwave synthesizers are required for many frequency-hopped satellite communication systems. These synthesizers must be of high-reliability design, of compact size, and light weight, in addition to having low DC power requirements.

This paper describes a space-flight qualified synthesizer system which meets these requirements and provides operational redundancy. The circuit technology utilized to implement an indirect synthesis technique using a VCO and phase-locked loop is described, together with circuitry for fast frequency switching, fine frequency tuning an control. The performance of major components is discussed in addition to overall synthesizer system performance."

[6] Bomford, M., "Analog Division Reduces Noise in PL Systems", MICROWAVES & RF, vol. 28, no. 4, pp. 98-110, April, 1989.

"Microwave frequency synthesizers that employ direct prescaling in a phase-locked loop (PLL) use analog or digital frequency dividers to downconverter signals. Although digital dividers offer small size and low cost, analog or parametric frequency dividers handle higher frequencies , consume less power, and generate less noise."

[7] Browne, J., "GaAs ICs: A "Short Form" Catalog of Standard Parts", MICROWAVES & RF, pp. 139-150, July 1988.

"The GaAs market is growing. Since the first GaAs IC Guide (see Microwaves & RF, December 1986, p. 135), analog and digital IC products have more than doubled. As a result, circuit and system designers have an unprecedented selection of "catalog" GaAs circuits from which to choose."

[8] Browne, J., "All-GaAs Lineup Fuels High-Speed Digital Synthesizer", MICROWAVES & RF, pp.128-136, July, 1988.

"Direct digital synthesis, renowned for low phase and fast switching speed, now includes broad bandwidth among its credits. The breakthrough comes in the form of the ADS-2 synthesizer from Sciteq Electronics (San Diego, CA), a 0.1-to-250-MHz synthesizer with astounding 20 ns frequency switching speed. The bandwidth is conservatively rated since the synthesizer runs on GaAs LSI ICs capable of clock rates in excess of 1 GHz."

[9] Ceracas, F.A.B., *et al.*, "A Hardware Phase Continuous Frequency Synthesizer for Frequency Hopping Spread Spectrum", MELECON 89: Mediterranean Electrotechnical Conference Proceedings. Integrated Research, Industry and Education in Energy and Communications Engineering, pp. 403-6, April 1989.

"One of the major problems when implementing Frequency Hopping Spread Spectrum (FH SS) systems is to obtain an accurate, fast and transient free frequency synthesizer. Direct Digital Synthesis (DDS) is an attractive technique to suit these requirements with economy and simplicity which is becoming increasingly widespread in a number of different areas and applications. A brief analysis of a direct frequency synthesizer is made indicating the several sources of noise that contribute to signal degradation, the frequency distribution of spurious due to phase and amplitude quantization and expressions for the signal-to-noise ratio. A hardware prototype was built (using ECL) and its performance is shown to be in good agreement with both theoretical and simulation results based on the computation of a FFT."

[10] Cheah, J.Y.C., "Low Cost Applications in Ku-Band Frequency Synthesis", Proceeding of the 2nd International Symposium on Recent Advances in Microwave Technology, pp. 498-501, 1989.

"Direct Digital Synthesis (DDS) frequency generation technique is fast becoming popular in synthesizing various signal modulation schemes in the digital communications domain. Its use in general commercial frequency synthesis applications is less favourable due to its implementation cost as compared with traditional phase lock techniques. However it can be shown that DDS based microwave frequency synthesis can lead to attractively low cost commercial applications. This paper describes the design of a Ku-band frequency synthesizer which takes advantage of the low step size allowed in the DDS technique and a low cost high power frequency multiplier design to achieve the frequency synthesis desired."

[11] Cowley, N., & I. Fobbester, "Refining the high speed divider", New Electronics, vol. 21, no. 1, pp. 50-1, Jan., 1988.

"The development of a frequency hopping synthesizer IC for multi-channel mobile radio."

[12] Eisenson, H., "Frequency-Hopping with Direct-Digital Synthesis", vol. 8, no. 13, pp. 33-4, Dec., 1985.

"Frequency synthesizers can be judged by any of several criteria and the relative weight of those parameters is determined by the application. In some cases, spectral purity is the overwhelming factor - in others it might be size alone. In every design situation, however, there is usually some combination of tradeoffs because no one methodology is ideal. In many technologies, including military communications and radar, one of the most important criteria is the speed with which the synthesizer can "hop" from one frequency to another, its switching speed."

[13] Galani, Z., & R.A. Campbell, "An Overview of Frequency Synthesizers for Radars", IEEE MTT, vol. 39, no. 5, May, 1991.

"This paper presents an overview of frequency synthesizer techniques suitable for radar systems. Included are the requirements which have a direct impact on the selection of synthesizer architectures and the choice of synthesizer components. Both direct and indirect architectures are presented, along with advantages, disadvantages, and representative examples. A brief discussion of analytical procedures is followed by a survey of key synthesizer components and future trends."

[14] Galani, Z., M.J. Bianchini, and J.A. Chiesa, "The Differential Reference Frequency Synthesizer", IEEE MTT-S Digest, pp. 1161-1163, 1991.

"Indirect digital frequency synthesizers cannot achieve fast frequency switching with closely spaced frequencies because of limitations imposed by the requisite narrow loop bandwidth. A novel dual-loop digital frequency synthesizer is presented which satisfies these conflicting requirements and, in most cases, exhibits improved phase noise performance."

[15] Gilmore, R., & R. Kornfeld, "Hybrid PLL/DDS Frequency Synthesizers", QUALCOMM Inc. internal report.

"This paper reviews the basic operation of the PLL synthesizer and the Direct Digital Synthesizer (DDS). After the basic principles are reviewed, techniques are described to combine the DDS and the PLL to create powerful hybrid synthesizers which can meet difficult performance specifications. Using the QUALCOMM Q2334 Dual DDS and the QUALCOMM Q3036 single chip PLL synthesizer, this hybrid synthesizer can be implemented using a minimal amount of circuity and power."

[16] Glance, B.S., "New Phase-Lock Circuit Providing Very Fast Acquisition Time", IEEE MTT, vol. MTT-33, no. 9, pp. 747-754, September, 1985.

"We present a new circuit configuration for second-order phase-lock loops that provides, for large initial frequency offsets, acquisition times several orders of magnitude shorter than those achieved using conventional phase-lock loops. This new circuit also provides frequency locking almost instantaneously when the time delay around the loop is small. Furthermore, it can, without losing lock, sustain frequency changes several hundred times faster than those which can be sustained by a conventional circuit."

[17] Kalivas, G.A., & R.G. Harrison, "Frequency Stability Characterization of Hopping Sources", 41st Annual Frequency Control Symposium, pp. 122-125, 1987.

"The increasing demand for Spread Spectrum (SS) Systems utilizing Frequency Synthesizers imposes a need for development of fast Frequency Hopping (FH) Systems which constitute the most important part of FH_SS or Hybrid-SS Communication Systems. Speed limitations of other systems suggests the employment of fast-tuning Voltage Controlled Oscillators (VCOs) which are digitally controlled through a Digital-to-Analog Converter (DAC). Since these sources are not phase-locked the output noise does not obey the PLL output noise formulation. Therefore an attempt is made here to use time-domain frequency stability measures to characterize the noise of this kind of free-running Hooping Sources."

[18] Gyenes, I., I. Valy, and T. Toth, "High-Speed Microwave Synthesizers", Proceedings of the Eigth Colloquium on Microwave Communication", pp. 79-80, August, 1986.

"Two kinds of fast switching microwave synthesizers have been developed, one to be used in burst and the other in frequency hopping communications systems. The first one is a single-loop system using high-frequency two-modulus prescalar frequency divider chain. The second one is a triple-loop divide-and-mix system employing high (1 MHz) reference frequency at the input of the PLL phase detectors. Both synthesizers use the same microwave circuits. The switching speed of the two synthesizers is less than 2 ms and 60 μs respectively. The first can be modulated directly with a 3 KHz - 6 MHz baseband signal. The output noise of both synthesizers is low enough to use them in digital communications systems."

[19] Harris, M.V., "A J-Band Spread-Spectrum Synthesizer Using A Combination of DDS and Phaselock Techniques", IEE Colloquium on Direct Frequency Synthesis, no. 172, pp. 8/1-10, Nov., 1991.

"The synthesizer described is for use in a spread-spectrum communication system where a high degree of immunity to interference is required. A frequency resolution of 100 Hz across an RF bandwidth of 2 GHz is achieved by the combination of two phaselocked loops (PLLs) with a relatively simple Direct Digital Synthesizer (DDS). The overall frequency resolution is determined by the frequency resolution of the DDS, which is potentially unlimited.

Decimal, or base-10 synthesis is obtained by using a decimal DDS, the design of which is outlined. By linearly ramping the DDS output frequency under digital control, it is possible to get sub-10 microsecond switching speeds with no cycle-slipping, with manageable PLL loop bandwidths (f_n of 700 kHz). The analysis is presented, together with detailed measurements of spurious levels from the DDS. Overall phase noise and spurious levels are presented."

[20] Hivkman I., "Putting DDS to work", Electronics World + Wireless World, vol. 98, pp. 937-41, Nov., 1992.

"The final part of Ian Hickman's series on direct digital synthesis considers the design possibilities provided by this new branch of RF technology."

[21] Jones, W.J., H.P. Benn, & J.G. Gardiner, "A Fast Hopping Synthesizer for Agile Radar", IEEE International Symposium on Circuits and Systems, vol. 3, pp. 2539-43, June, 1988.

"This paper describes a direct synthesizer that combines direct analogue and digital techniques to produce a low noise fast switching X-band source. Direct digital frequency synthesis performance is terms of spurious content is described."

[22] Jones, W.J., & J.G. Gardiner, "Microwave Frequency Synthesis Using Mixed Analogue and Digital Techniques", International Conference on Frequency Control and Synthesis, pp. 139-44, April,1987.

"This paper describes a direct synthesizer currently under development that combines both direct analogue and direct digital synthesis to produce a fast hopping low noise coherent source for an X-band radar. The prototype synthesizer was conceived with a view to incorporating future innovations in MMIC and VHSIC technologies and was therefore built in modular form with each building block being capable of integration."

[23] Kajiwara, A., & M. Nakagawa, "A New PLL Frequency Synthesizer with High Switching Speed", IEEE Transactions on Vehicular technology, vol. 41, no. 4, pp. 407-413, Nov., 1992.

"In this paper, a new phase locked loop (PLL) frequency synthesizer with high switching speed is proposed, and the experimental and theoretical results are given. Mobile communication networks are evolving towards micro-cellulars operating in narrowband TDMA and microwave bands to meet the rapidly increasing demands for both voice and data services. Therefore, synthesizers with high switching speed are required for the realization. However, it will be difficult for conventional synthesizers to provide the switching time of shorter than 1 ms. The PLL synthesizer proposed here is composed entirely of digital signal processors except for a voltage-controlled oscillator (VCO). The VCO control signal is derived by the subtraction of the linear reference phase and the feedback phase, therefore, it does not need the band-limited loop filter which limits the ability of the loop to switch fast. The experimental results show that it can provide switching time as short as 0.1 ms, which is $10^2 - 10^3$ times higher than conventional PLL synthesizers, and spurs of less than -60 dB."

[24] Kasiwara, A., & M. Nakagawa, "PLL Synthesizer for Fast Frequency Hopping Spread Spectrum Communication", Electronics and Communications in Japan, Part 1, vol. 74, no. 1, pp. 105-114, 1991.

"This paper proposes a new PLL synthesizer for fast frequency hopping communications. The proposed synthesizer is composed entirely of digital signal processing circuits, except for the voltage-controlled oscillator. The phase comparator subtracts the phase of the reference and the feedback signals to produce the phase error signal. By this scheme, no harmonic or nonlinear distortion component is generated as in the conventional PLL synthesizers. Consequently, the loop filter is eliminated, resulting in a stable frequency synthesis with fast acquisition speed.

This paper examines the performance of the proposed method by simulation. It is verified that the frequency acquisition speed is improved by a factor of 10^3 to 10^4 compared with the conventional method, which is a drastic improvement."

[25] Kimbrough, L.W., "Choosing the Optimum Synthesizer Architecture for Your Receiver Application", Proceedings. RF Expo East, pp. 203-15, Sept., 1992.

"Synthesizer design is driven by 6 basic parameters; 2 are fixed, the other 4 are usually somewhat flexible depending on other system tradeoffs. The fixed requirements are Output Frequency and Frequency Step Size. The flexible parameters are: Phase Noise, Output Spurious, Settling Time, and Size/Power. The relative flexibility of these 4 parameters will depend on the specific application and the overall System Requirements. For example in a battery powered hand-held radio, the size/power is fixed and phase noise and spurious specs may simply be "as good as possible". But in a rack mounted intercept receiver, the phase noise may be spec'ed at state-of-the-art performance with no limits on size/power parameters. The complexity of the synthesizer's implementation is related to the difficulty of each of the 4 flexible parameters. The 2 fixed parameters will typically dictate a complexity that will increase with increasing Output Frequency and decreasing Step Size. This paper takes a synthesizer spec and derives the performance for 6 basic synthesizer architectures, all of which meet the fixed requirements but meet the 4 flexible requirements according to implementation. This process may be applied to any Receiver application. For the purpose of comparison, the example used is an HF Receiver's Local Oscillator."

[26] Kolumban G., "A Simple Frequency Synthesizer Configuration for Low Capacity Digital Microwave Radio Links", Conference Proceedings. 21st European Conference, pp. 1453-8, Sept., 1991.

"A new low cost frequency synthesizer configuration has been developed for a low-capacity digital microwave radio equipment. The key element of the proposed synthesizer configuration is a double sampling SPLL circuit. The paper gives the exact model of the double sampling SPLL, determines the conditions for stability and develops the equations describing the modulation properties of the circuit. The theoretical results will be verified by measured data."

[27] Kolumban G. "A Fast Frequency Synthesizer for FH Systems",Proceedings of the eighth Colloquium on Microwave Communication, pp. 253-4, Aug., 1986.

"The exact system equations of the sampled PLL's using one or two sample and hold circuits are given. The models take into account the characteristics of the realizable sampler circuits. The stability properties of the loops and the conditions of the minimum frequency switching time are also investigated."

[28] Kuge, J., T. Iritani, & T.Oie, "Fast Hopping Frequency Synthesizer with Small Frequency Error", IEEE International Conference on Selected Topics in Wireless Communications. Conference Proceedings, pp. 215-18, June, 1992.

"In Frequency Hopping Spread Spectrum (FH-SS) communication, the ability of the frequency synthesizer is required to switch the carrier frequency quickly. But, if a conventional PLL is used as a component of the synthesizer, high speed frequency switching is not expected because of the time constant of PLL.

In this paper, we propose new type synthesizer independent on the above time constant, and we described the experimental results."

[29] MacConnell, & R.W.D. Booth, "A Feedback Method for Reference Spur Reduction in PLLs", RF Design, pp. 50-53, Sept., 1990.

"This paper describes a circuit that is extremely useful in reducing reference sidebands in phase locked loops or indirect frequency synthesizers which are caused by reference leakage from the active phase/frequency comparator. In excess of 40 dB reduction in reference spurious signals is routinely achieved without any impairment in loop dynamics due to spur reduction filters. The benefit of this circuit is that the necessary filtering required to obtain a given spurious signal level may be considerably reduced, especially in loops containing large division ratios such as microwave frequency synthesizer. In some cases, it has been impossible to achieve the desired spur level without the use of this circuit."

[30] Morris, G., "Microwave indirect synthesis", Microwave Engineering Europe, pp.31-35, August/September, 1991.

"Gordon Morris from M/A Com, Dunstable, UK describes synthesis techniques that have been developed to provide -120 dBc/Hz phase noise and 5 µs channel switching. Examples described include phase locked direct synthesis and a dual synthesizer at L band."

[31] Naber, J.F., *et al.*, "A Fast-Settling GaAs-Enhanced Frequency Synthesizer", IEEE Journal of Solid-State Circuits, vol. 27, no. 10, pp. 1327-31, Oct., 1992.

"An indirect, phase-locked loop (PLL) GaAs-enhanced frequency synthesizer with 700 ns loop settling time has been developed. The two-chip GaAs insertion reduced the size of an existing synthesizer from 90 in^3 to only 30 in^3. The 6.0 x 5.5 x 0.9-in module contains a 400-gate GaAs programmable divider and a sample and hold (S/H) which improved the settling time 77% and reduced the size 67% over the current state-of-the-art synthesizer. Furthermore, the divider reduce power dissipation by 9.7 W and the S/H reduced power dissipation by 1.3 W."

[32] Nuchter, P., & W. Menzel,"A MM-Wave Frequency Divider", IEEE MTT-S Digest, pp. 695-697, 1992.

"At lower GHz frequencies, frequency dividers are widely used - in conjunction with PLL circuits - for frequency stabilization. This was, up to now, difficult for mm-wave frequencies. This paper presents, for the first time, a mm-wave frequency divider with a division ratio sufficiently high (e.g. 8) so that digital dividers can be used next. The mm-wave divider is based on a combination of analogue and digital components, and it may easily be realized using (monolithically) integrated circuits."

[33] Osafune, O., & K. Ohwada, "Ultra-High-Speed GaAs Monolithic Prescaler and Phase Frequency Comparator IC", IEEE MTT, vol. MTT-34, no. 7, July, 1986.

"A high-speed, low-power prescaler and phase frequency comparator (PFC) IC for a phase lock stable oscillator was designed and fabricated on a single chip using GaAs MESFET BFL circuitry. The gate width of the master-slave T-type flip-flops used in designing the 1/32 frequency divider prescaler was determined by circuit simulations. The fabricated 1/32 prescaler operated up to 8.0 GHz while the fabricated monolithic prescaler and PFC IC performed stable division, and phase and frequency comparison at input frequencies up to 4.8 GHz with a chip power dissipation of only 715 mW."

[34] Perez, J., *et al.*, "Application of Harmonic Dividers to Frequency Synthesizers in Millimeter Band", Proceedings of MELECON '87: Mediterranean Electrotechnical Conference and 34th Congress on Electronics Joint Conference, pp. 361-4, March, 1987.

"This paper describes the design and realization of frequency dividers by harmonic injection, to be used in frequency synthesizers, which are one of the most important parts in a K band (22 GHz) digital radio-link. Three different dividers are presented with a brief description of their design and the experimental results obtained."

[35] QUALCOMM Application Note entitled "Hybrid PLL/DDS Frequency Synthesizers".

"This application note shows how to design hybrid PLL/DDS circuits that eliminate the tradeoffs and give new designs "the best of both worlds" in terms of bandwidth, resolution, switching time, noise and circuitry. Table 1, Comparison of Frequency Synthesizers, shows that hybrid circuit designs using the QUALCOMM Q2334 Dual DDS and Q3036 1.6 GHz PLL chips outperform individual PLL of DDS designs."

[36] Ress, B.,"Prescaler Aids Design of Fast Frequency Source", MICROWAVES & RF, pp. 129-131, Nov., 1990.

"Indirect microwave synthesizers usually incorporate frequency downconversion prior to phase comparison of oscillator and reference signals. Traditionally, downconversion is executed by harmonic sampling or heterodyne mixing techniques. But the availability of inexpensive, digital frequency dividers offers microwave designers a simpler option for high-performance indirect-synthesizer architectures."

[37]. Seki, K., M. Morikura, & S. Kato, "High Resolution and Fast Frequency Settling PLL Synthesizer", IEICE Transactions on Communications, vol. E75-B, no. 8., Aug., 1992.

"This paper proposes a high resolution and fast frequency settling PLL synthesizer for frequency hopping radio communication equipment. The proposed synthesizer enables the carrier freqeuncy to be changed within the duration of a burst signal and yields higher frequency resolution than the reference signal frequency. To reduce frequency settling time without degradation of frequency resolution and phase noise, this paper proposes a new phase and frequency preset (PFP) PLL synthesizer which employs a digital phase accumulator to generate high resolution reference signal. Experimental results show that the settling time of a prototype synthesizer is less than 300 µs while spurious signals are suppressed by more than 55 dB. In comparison with conventional PLL synthesizers, the frequency settling time is reduced by 80%. Furthermore, the higher frequency resolution than the reference signal is successfully demonstrated. Therefore, the proposed PFP PLL synthesizer with the digital reference signal can achieve the output signal with high frequency resolution less than 1 Hz."

[38] Shigaki, M., "Study on GaAs Monolithic Divider", Electronics and Communications in Japan, Part 2, vol. 71, no. 4, pp. 44-49, 1988.

"The GaAs monolithic dynamic divider, a high speed divider for microwave phase locked oscillators, has been studied. It can be operated at a higher speed than static dividers. The load in the inverter section is a passive resistor. Improved circuit topology at interstage buffers and reduction of gate resistance by the Au/WSi self aligned process have been used for superior characteristics of a single FET. For a 1 µm gate length, both division and frequencies ranging from 4.3 GHz to 7.3 GHz have been observed. As a system application, the divider has been implemented in a 13 GHz frequency synthesizer of oscillator-multiplier type. The divider has been operated in the 6.5 GHz band and an operation with 1 MHz steps has been confirmed at the 13 GHz band. The phase noise has been 90 dBc/Hz at the off-carrier frequency of 10 kHz. This value is sufficient for conventional microwave circuits."

[39] Stanley, T., "The RF Design Revolution", Electronics World + Wireless World, vol. 98, pp. 999-1003, Dec., 1992.

"Frequency generation is at the heart of RF design. Virtually all radiocomms systems operate on channelised frequency allocations. Demands on the spectrum require that frequency slots must be re-used; frequency agility is a must for user equipment. Only frequency synthesis can provide this."

[40] Stilwell, J. "A Flexible Fractional-N Frequency Synthesizer for Digital RF Communications", RF Design, pp. 39-43, Feb., 1993.

"In digital RF communications systems, typical single-loop synthesizers may not meet all switching time, noise and spurious output requirements. An introduction to fractional-N frequency synthesis and a comparative evaluation between standard and fractional-N single-loop synthesizers in a 900 MHz application are presented. A simple passive fitler design procedure, information on loop analysis and optimization using commercially available software and design tips are also included."

[41] TRIQUINT data sheet entitled "TQ6122 8-Bit, 1 Gs/s, Digital-to-Analog Converter", REV. A.3, Oct., 1992.

"TriQunit's TQ6122 GIGADAC^{TM} is a monolithic 8-bit GaAs Digital-to-Analog Converter capable of conversion rates to at least 1000 Megasamples/second. This DAC may be used for display generation, waveform and signal synthesis, and video signal reconstruction, and features a 2:1 data MUX at the input for ease of interface. The DAC offers synchronous blanking capability for maximum ease of use in video applications, and is designed to drive complementary 1 V peak-to-peak swings into 50 ohm loads; extremely fast settling time is provided by on chip 50 Ω reverse terminations."

[42] Tsimbinos, J., "The Use of Direct Digital Synthesizers and Phase Locked Loop Frequency Multipliers for Generating Local Oscillator Signals in Digital Radios", IREECON '91: Autstralia's Electronics Convention Proceedings, vol. 2, pp. 546-9, 1991.

"Direct digital synthesis is being recognized as an alternative to conventional phase locked loop frequency synthesis. A discussion on its use with phase locked loop frequency multipliers for generating high frequency local oscillator signals is given. Methods of calculating the spurious noise are explained. Details of a synthesizer design example are presented."

[43] Vulcan, A., & M. Bloch, "A Low Noise Vibration Isolated Airborne Radar Synthesizer", IEEE Proceedings of the Forty-Fifth Annual Symposium on Frequency Control", pp. 330-335, May, 1991.

"A ku-band synthesizer is described which incorporates both direct and indirect techniques to generate exceptionally pure signals with low phase jitter and spurious content. Fast switching speed and phase noise of -120 dBc/Hz from 10 kHz to 40 MHz is obtained. The radar operates in a fighter aircraft environment that has a high level of random vibration and static G loading, and the mechanical design incorporates vibration isolation techniques. The master oscillator, from which the various fixed and steppable frequency outputs are derived, uses a low G sensitivity SC cut crystal. Ku-Band phase noise performance data is presented and the correlation between anticipated and measured performance is discussed."

[44] Walls, F.L., & C.M. Falton, "Low Noise Frequency Synthesis", IEEE Proceedings of the 41st Annual Frequency Control Symposium, pp. 512-18, May, 1987.

"This paper reviews the various definitions of phase noise and changes in the phase noise of a signal under noiseless multiplication, division, and translation. Next the phase noise in selected non-cryogenic rf and microwave oscillators is reviewed. Using a systems approach one can synthesize a microwave signal where the close in phase noise is controlled by a microwave source. This approach yields a phase noise performance that is superior to that possible with a single source. Finally the phase noise of various amplifiers, multipliers, and dividers is compared. The phase noise of dividers while generally inferior to that of the best multipliers, is often sufficient of most applications. Special note should be made that the phase noise quoted in the literature for some dividers is perhaps pessimistic and that the phase noise quoted of the system will often be seriously affected if placed under vibrational or thermal stress."

[45] Weiss, F., & T.G. Bowman,"A 14-Bit, 1Gs/s DAC for Direct Digital Synthesis Applications", IEEE GaAs IC Symposium, pp. 361-364, 1991.

"A GaAs digital to analog converter having 14-bit resolution and >1 Gs/s sampling rate is described. The device is intended for use in direct digital synthesizer applications and exhibits a typical untrimmed DC differential nonlinearity of 0.1% F.S., corresponding to a -60 dBc spurious-free dynamic range when used to generate a 12-bit resolution sinewave at a sampling rate of 750 Ms/S. The maximum sampling rate is 2 Gs/s. The circuit utilizes on-chip current sources, dissipates 2.5 watts, and is packaged in a custom multilayer ceramic package."

[46] Williams, D.A., "The Use of Digital Techniques in Indirect Microwave Frequency Synthesizers", IEE Colloquium on Applications of Digital Techniques in Microwaves, no. 130, pp. 7/1-9, Dec., 1986.

"The advent of high performance digital integrated circuits has had a tremendous impact in the field of Microwave Signal Sources. It is now possible to construct digitally programmable Signal Sources capable of generating many discrete frequencies having high levels of long and short term stability. This paper discusses the use of digital techniques in various sections of a Fast Switching Microwave Synthesizer and describes how circuits from various logic families (TTL, ECL and CMOS) have been used together in a single system making best use of their individual characteristics."

[47] Willamson, I.M.H., P.J. Webb,& P.W. Chilvers, "An Advanced Indirect Microwave Synthesizer",Conference Proceedings. Military Microwaves '90, pp. 220-8, 1990.

"This paper describes how the exacting requirements now being place on synthesizer manufacturers for advanced radar systems can be satisfied. These requirements include not only improved performance, but also shorter development timescales within ever shrinking development budgets.

As an example the paper gives details of an X-band synthesizer developed for an airborne radar which demanded very small size, extremely low phase noise, fast frequency switching and short development timescales.

In meeting the technical requirement, full use was made of a proven Phase Locked Direct Synthesis approach. This technique combines analogue Direct Synthesis using comb generators and switched lumped element filters with Indirect Synthesis or Phase Locked Loop techniques.

The greatest challenge lay in meeting the small size and called upon extensive use of hybrid circuitry and advanced packaging techniques. A building block approach readily lent itself to size reduction and resulted in a new generation of synthesizer building blocks being established for future programs."

[48] Wolfson, H.M., "A Very Small Frequency Generator System for Spread Spectrum EHF Applications", IEEE, 1989.

"The paper reports on a novel synthesizer architecture, utilizing a hybrid Direct Digital/Direct Analog approach, which was optimized for small size, fast tuning, low spurious and low phase noise for a hopping EHF terminal. Performance data of the completed Frequency Generator System is presented which shows 500 nanosecond frequency switching speeds over a 600 MHz tuning bandwidth centered at 11.1 GHz, with 2.2 Hz resolution. Single-sided phase noise, L (f), is less than -80 dBc/Hz at a 1 kHz offset from the 11 GHz output and the worst case spurious is -40 dBc. The complete unit was packaged in 72 cubic inches, weighs 3.0 pounds and requires 16.5 Watts of DC power during continuous operation. This frequency generator demonstrates a vast improvement over any other reported synthesizer implementations for EHF systems."

[49] STANFORD TELECOM (1990). "1-GHz GaAs 32-Bit Modulated Numerically Controlled Oscillator STEL-2173", The Spread Spectrum Handbook (1990), pp.37-64.

"The STEL-2173 is a GaAs Modulated Numerically Controlled Oscillator (MNCO) which operates at clock frequencies up to 1 GHz and uses digital techniques to provide a cost-effective solution for precision very high frequency signal sources. This monolithic device is ideal for use in frequency synthesizers, frequency hoppers, and other precision frequency sources. It has a frequency resolution of 32 bits, making it possible to generate signals from 0 to more than 400 MHz with a resolution of 0.23 Hz."

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This report describes the results of a detailed study into the development of an EHF STACOM payload frequency-hopping synthesizer. The synthesizer is required to provide an output between 20.2 GHz and 21.2 GHz, in steps of up to 200 Hz, with a switching time of less than 900 nanoseconds. A literature review of the various synthesizer architectures was conducted and used to devise three possible synthesizer solutions. These three solutions were then compared on the basis of a number of key criteria. The preferred synthesizer, of the three, will provide the required output in steps of 0.92 Hz, with a switching time of 100 nanoseconds. The various characteristics of the preferred synthesizer are described in detail. The viability of implementing a design using the preferred synthesizer approach is discussed. Finally, a specification sensitivity analysis of the selected synthesizer approach is performed.

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